



**The Abdus Salam
International Centre for Theoretical Physics**



2065-17

**Advanced Training Course on FPGA Design and VHDL for Hardware
Simulation and Synthesis**

26 October - 20 November, 2009

**VHDL & FPGA Architectures
Programmable Logic and VHDL Architectures**

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Lectures: VHDL & FPGA Architectures



- Introduction to FPGA & FPGA design flow
- Synthesis I - Introduction
- Synthesis II - Introduction to VHDL
- Synthesis III - Advanced VHDL
- Design verification and timing concepts
- Programmable logic & FPGA architectures
- Actel ProASIC3 FPGA architecture
- System-on-Chip concepts



Programmable Logic and FPGA Architectures



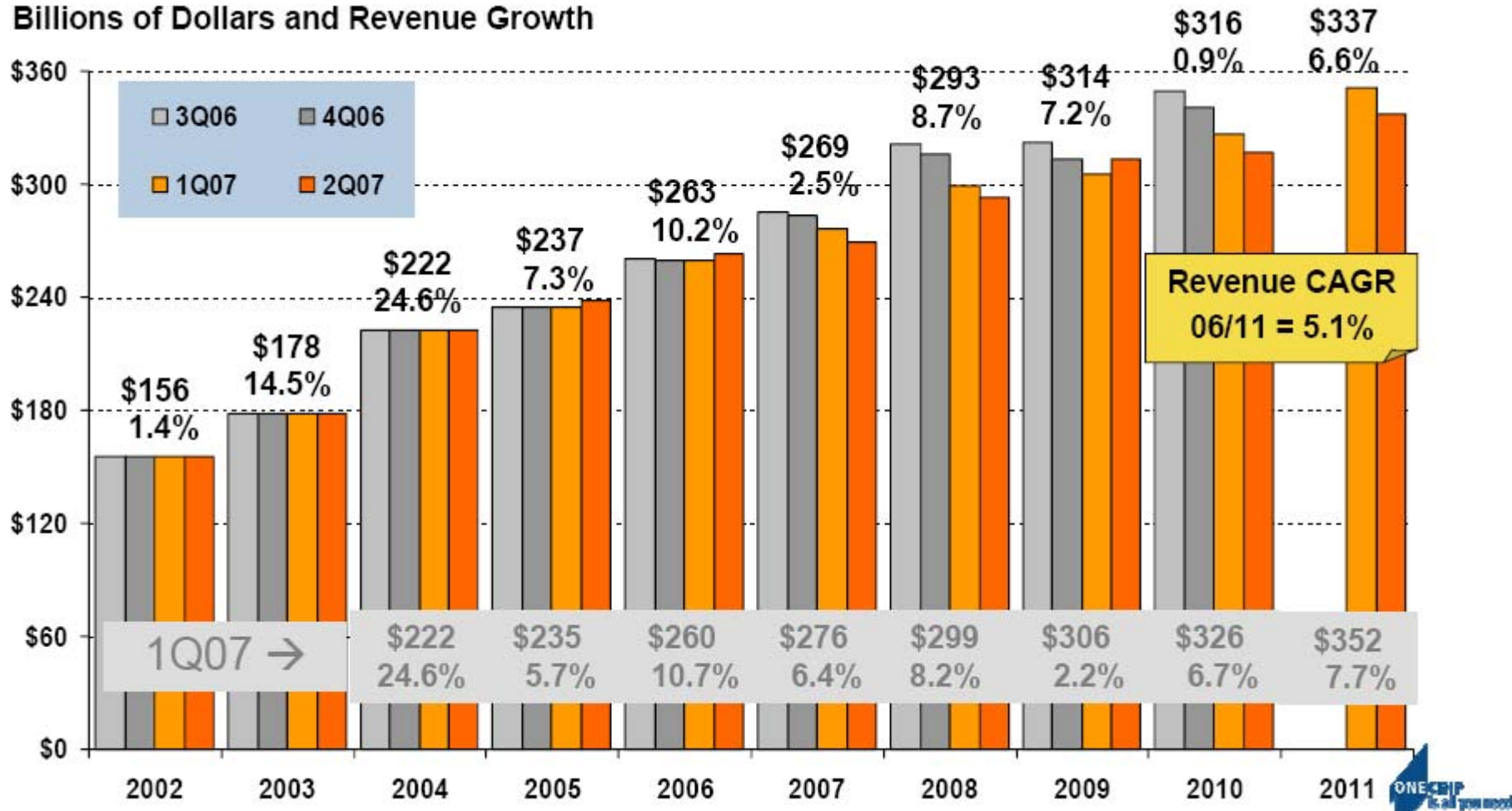
It's All About the Original Idea



PLD Market Growth



Billions of Dollars and Revenue Growth



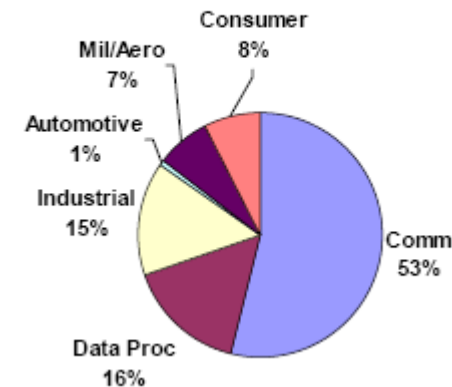
Source: Gartner Dataquest Estimates (May 2007)

- New adopters are in high volume segments
 - **Consumer grows from 8% to 15%**
 - **Automotive grows from 1% to 6%**

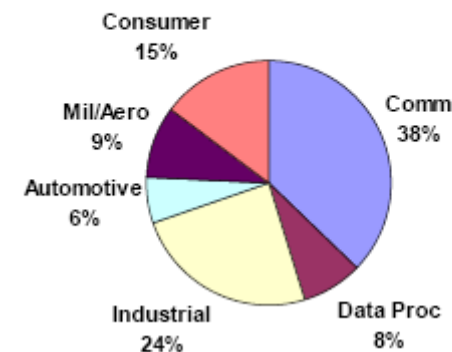
- Traditional ASIC-crossover segments also growing well
 - **Industrial is up 9%**
 - **Mil/Aero is up 2%**

- While high-end FPGA markets decline in share
 - **Comm down 15% in share**
 - **Data proc down 8% in share**

2002 PLD TAM - \$2.3B

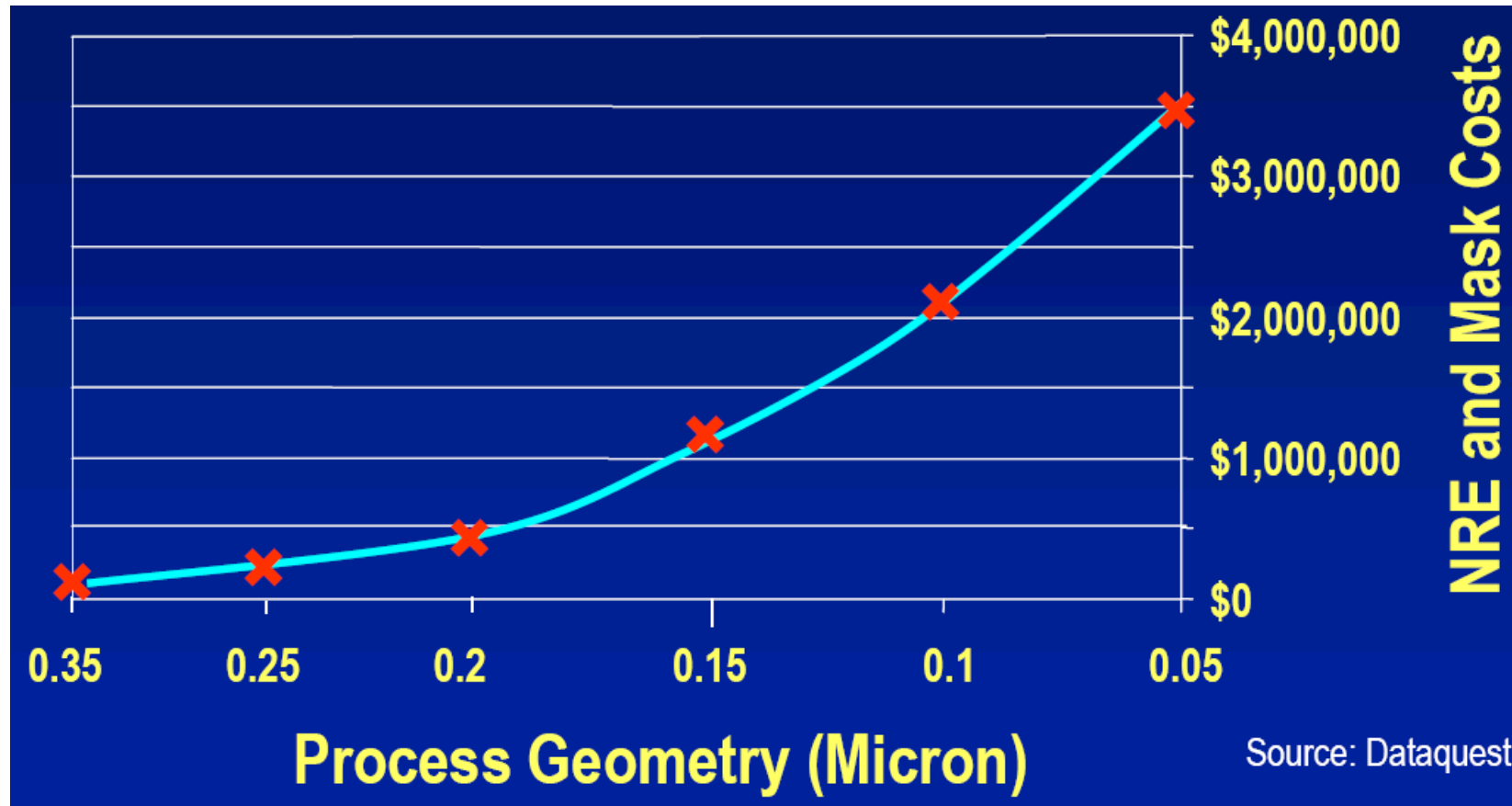


2010 PLD TAM - \$6.7B

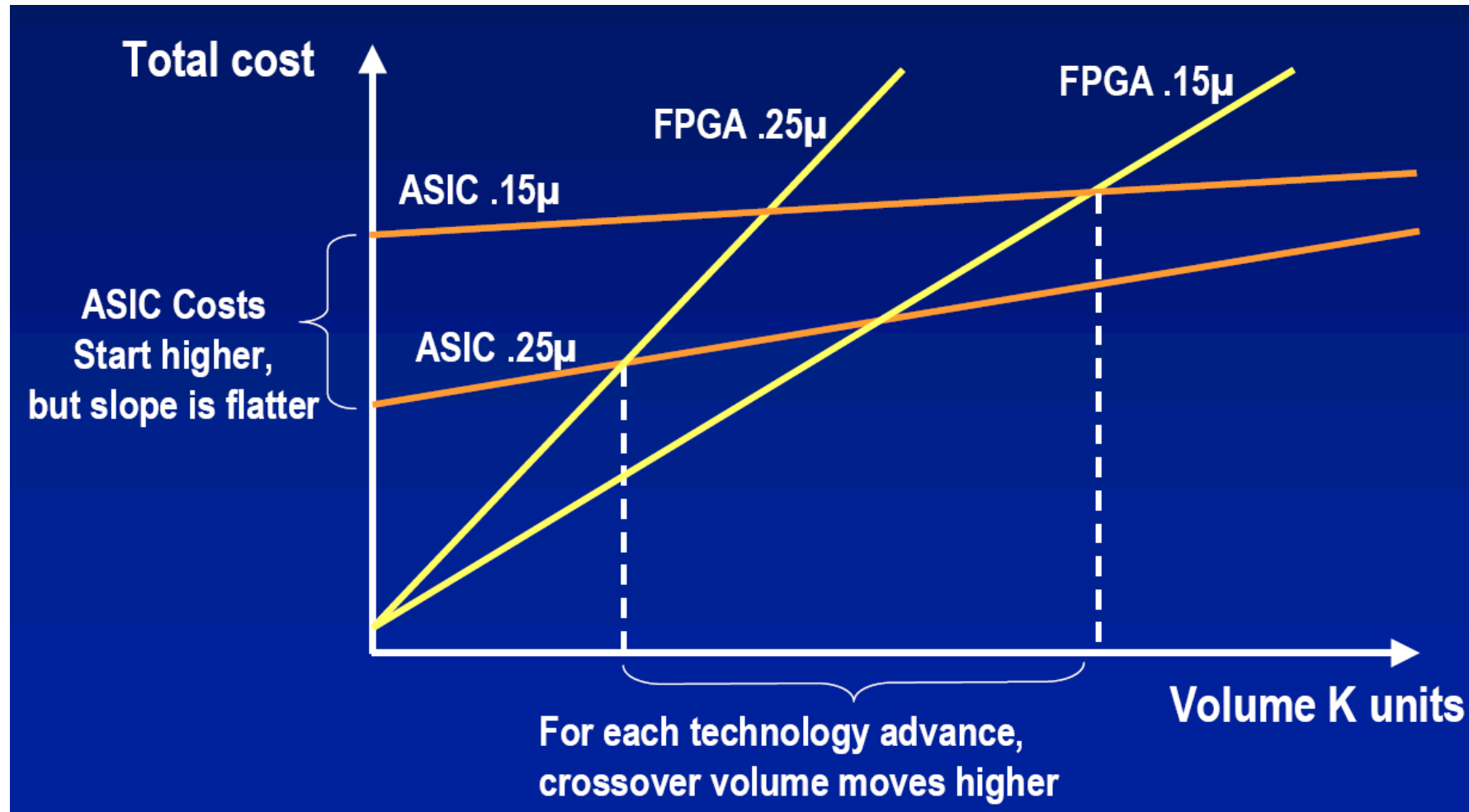


- Wafers today are worth from US \$10 million to \$100 million
- Amortize the \$5 billion investment in a fab over a 5 year schedule costs > \$3 million/day
- Equipment running all the time
- Must produce a semiconductor product in volumes of at least 5000 to 10 000 wafers per month

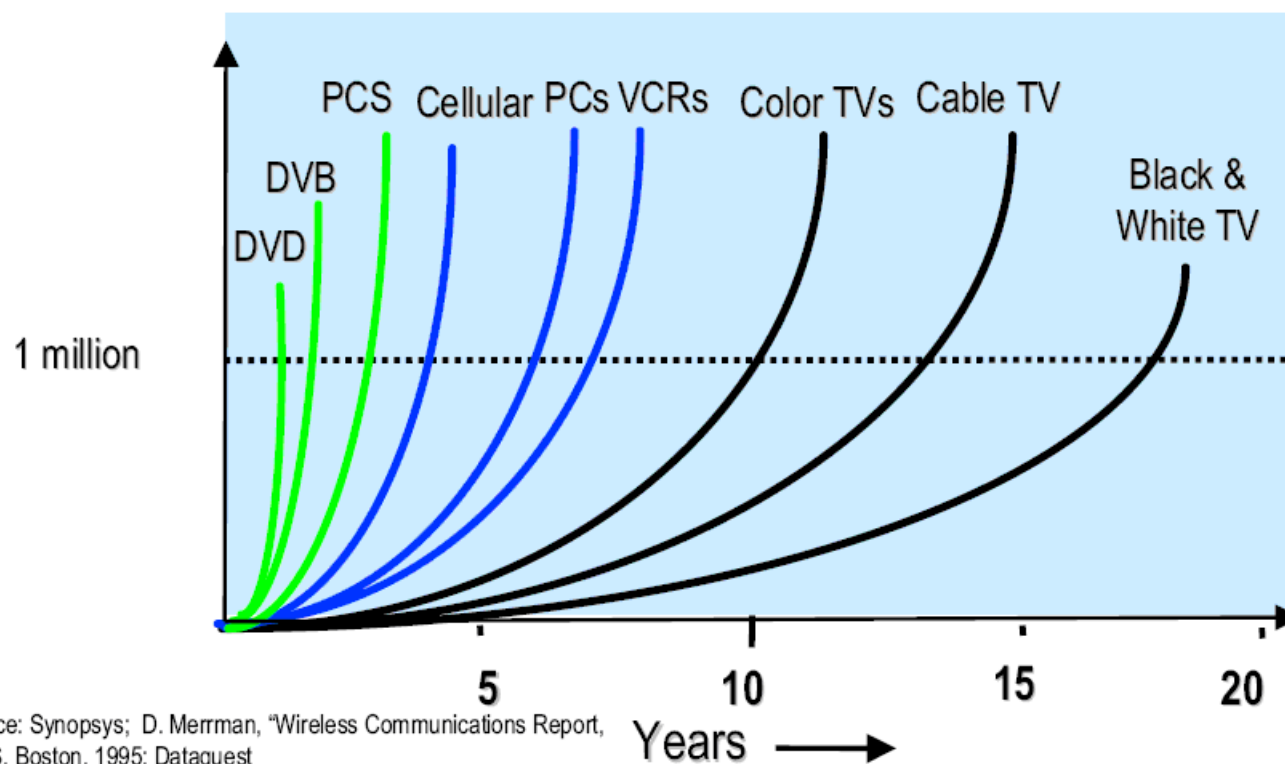
Cost: The exploding ASIC NRE



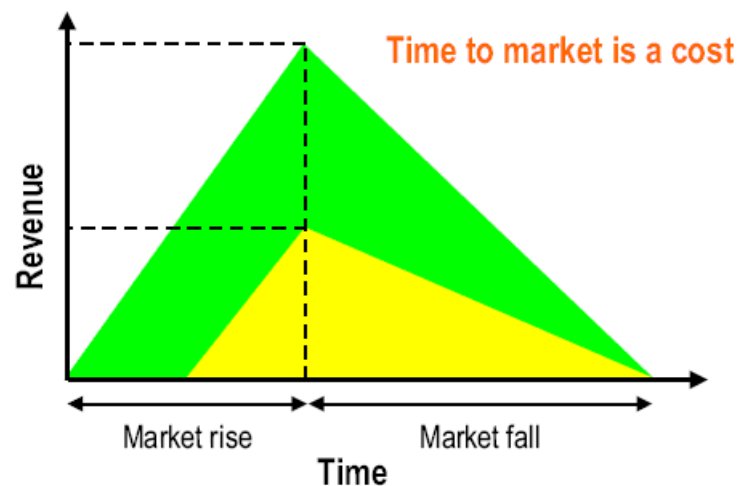
Technology Advances vs. Crossover Volume



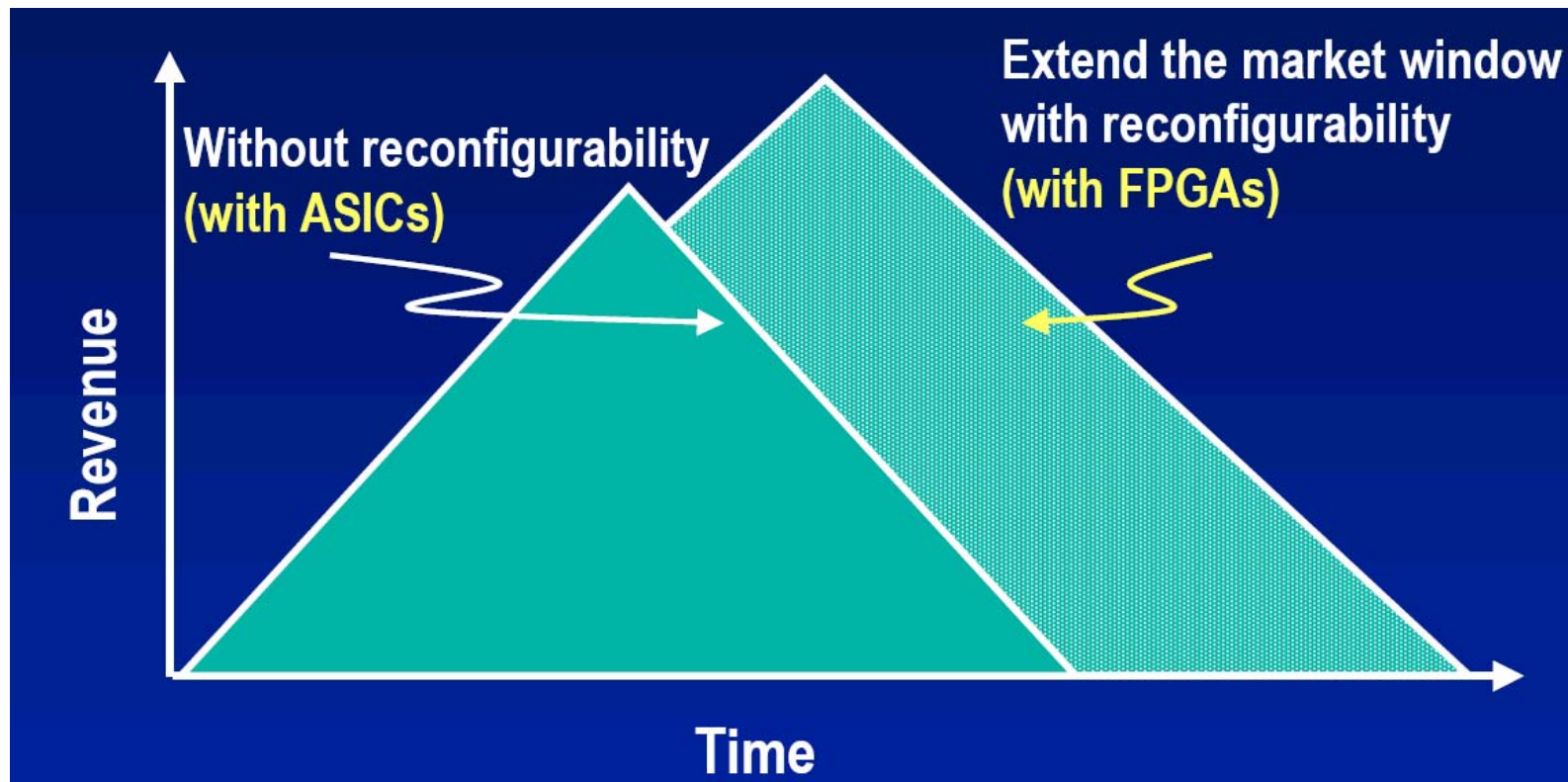
New products are taking less time to go into volume. At the same time, new products also stay in volume for shorter

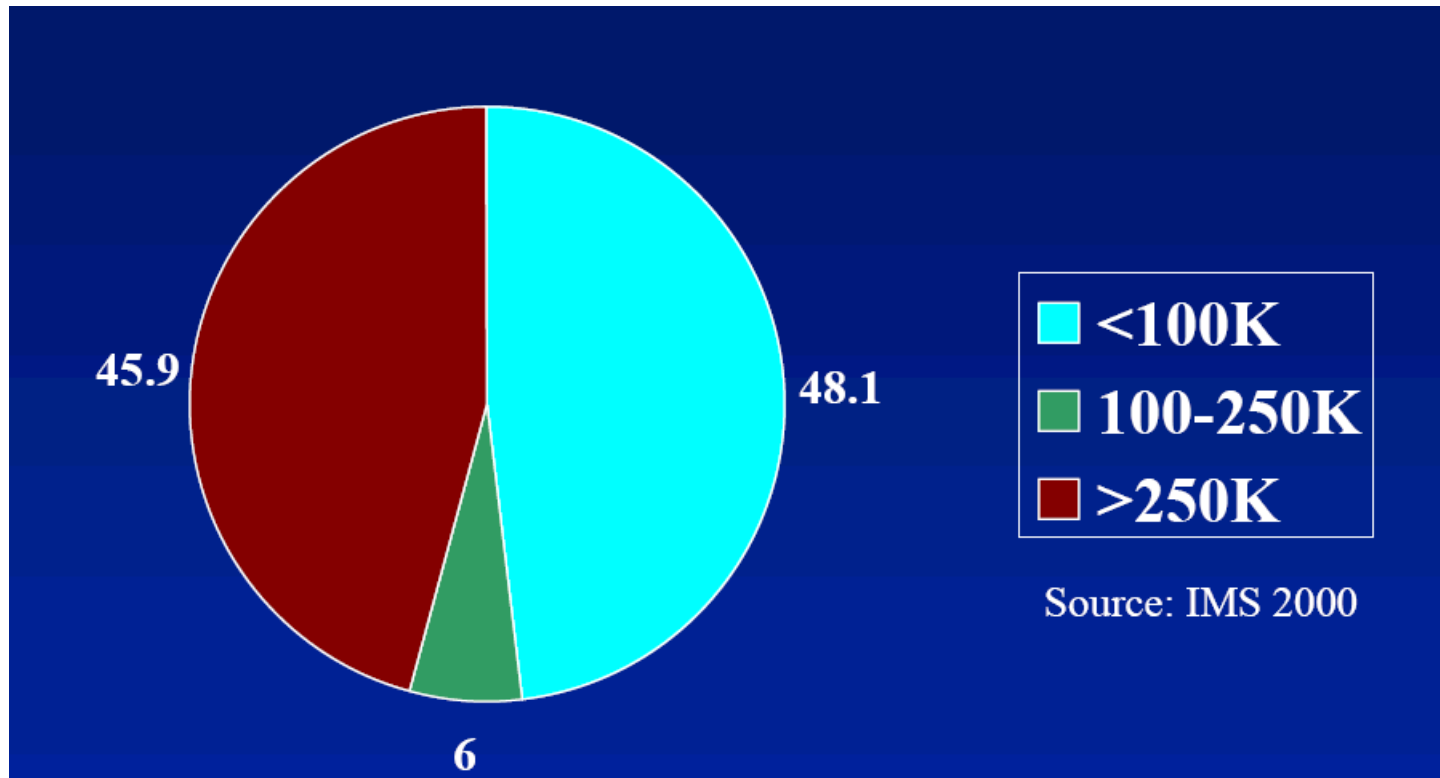


- ❑ Missing a market window, because of a long development/debugging cycle can have a profoundly negative effect on the profitability of a product over its life..
- ❑ Late market entry has a larger effect on profits than development cost overruns or a product price that is high.

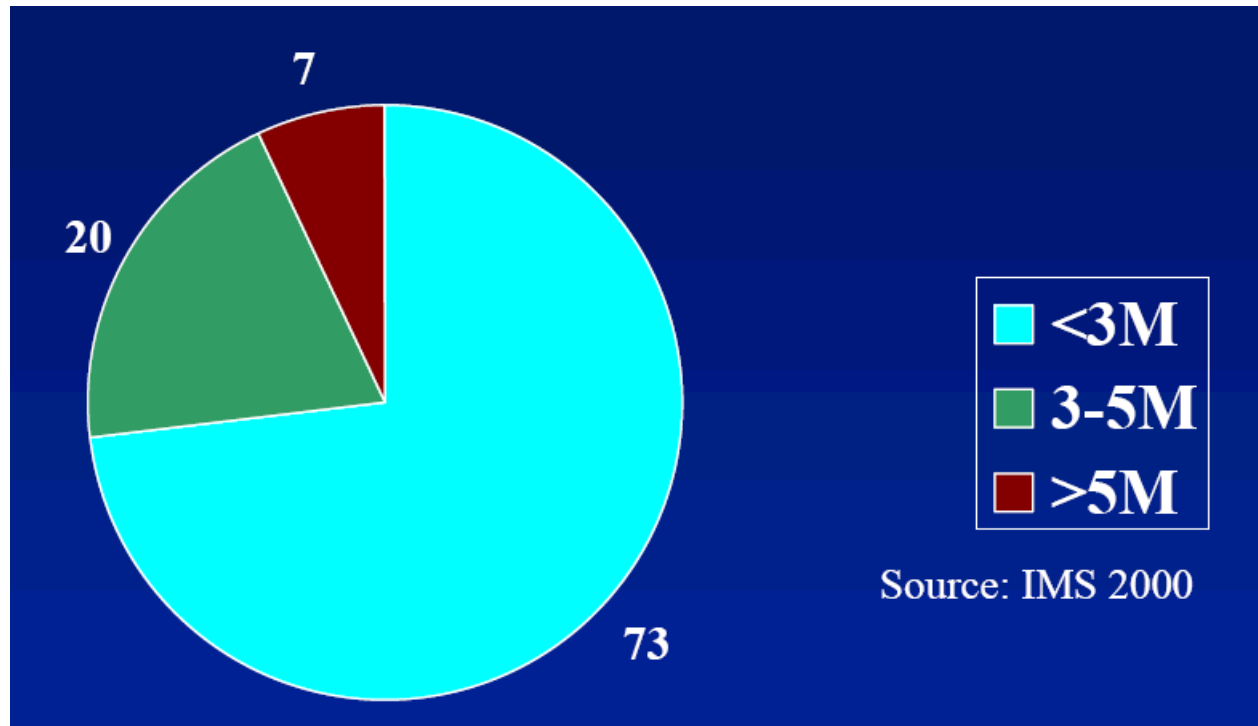


- ❑ Lack of re-configurability in ASICs is a huge opportunity
- ❑ FPGAs offer flexible life cycle management

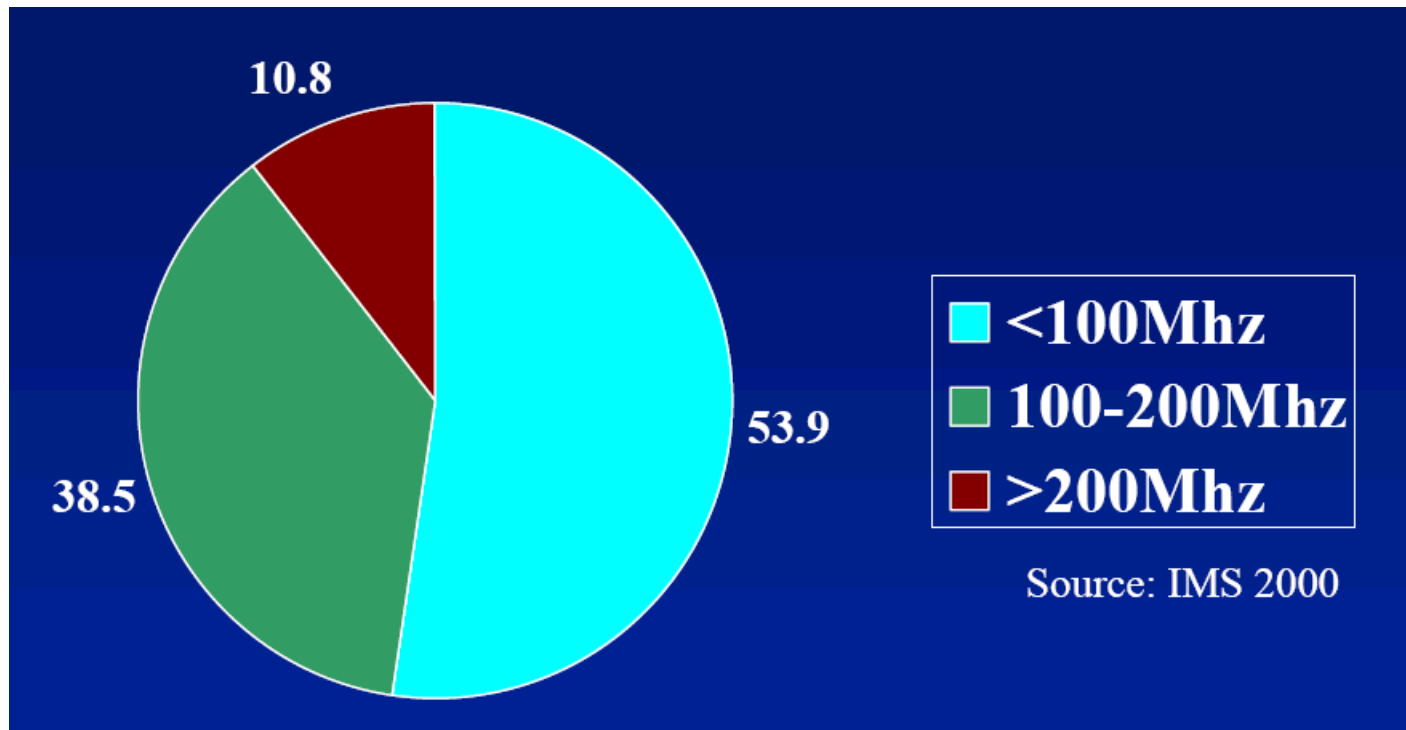




- > 50% of the market available today for FPGAs



- FPGA can address a very large part of the market today

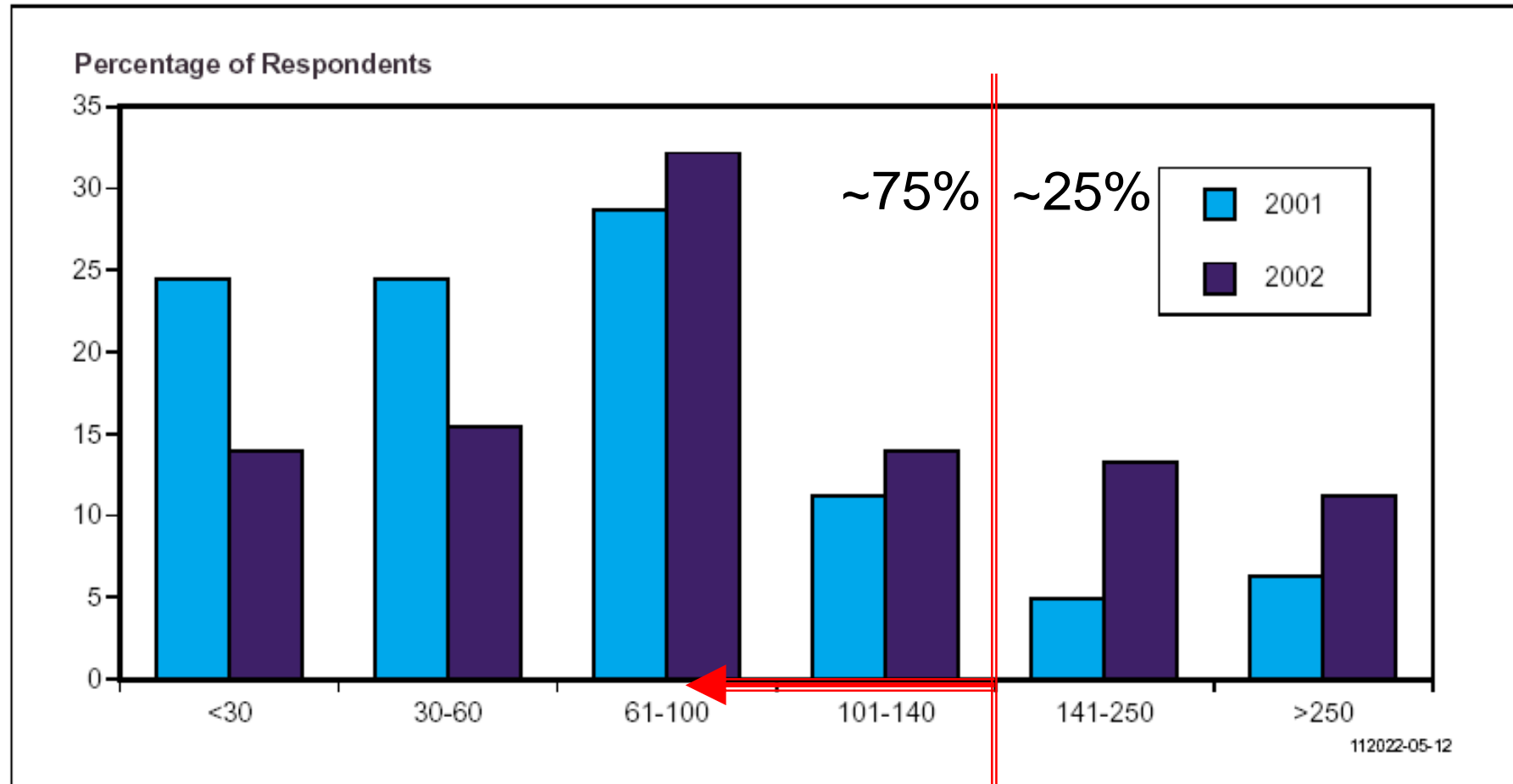


- FPGA can address a very large part of the market today

Performance Requirement for FPGAs



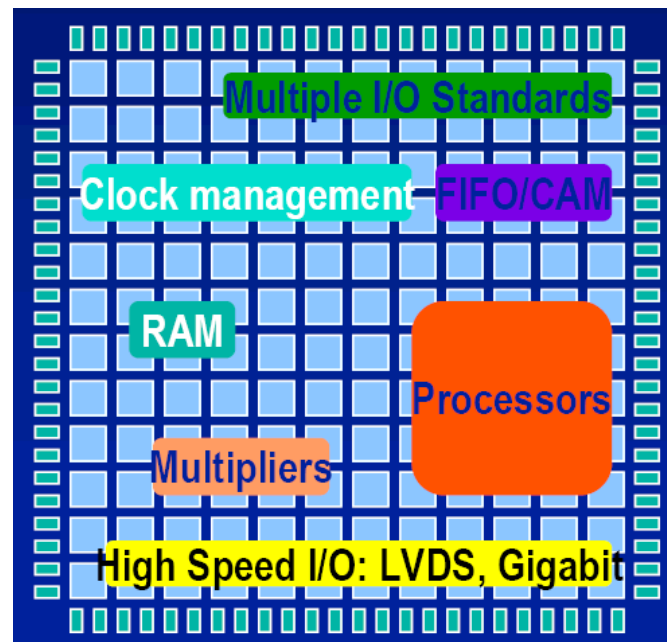
Maximum On-Chip Clock Frequencies (Megahertz) — FPGA Design Starts



Source: Gartner Dataquest (January 2003)

- FPGA can address a very large part of the market today

- 7 years ago, FPGAs were only gates & routing
~25000 gates
- Today, there are several system-level features.
~5,000,000 gates
- The trend to add more IP in FPGAs continues



Once upon the time, there were... ROMs:

- ✘ Expensive

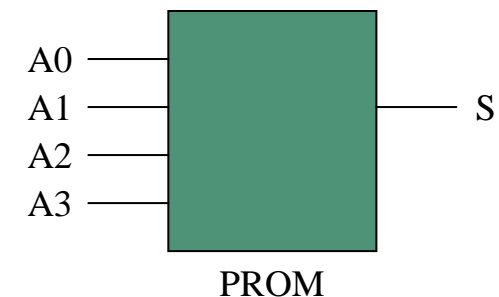
- ↪ Need for creating an application specific mask set by the vendor

- ✘ Long development cycle

- ↪ Changes = New mask set by the vendor

PROMs: Programmable Read Only Memories

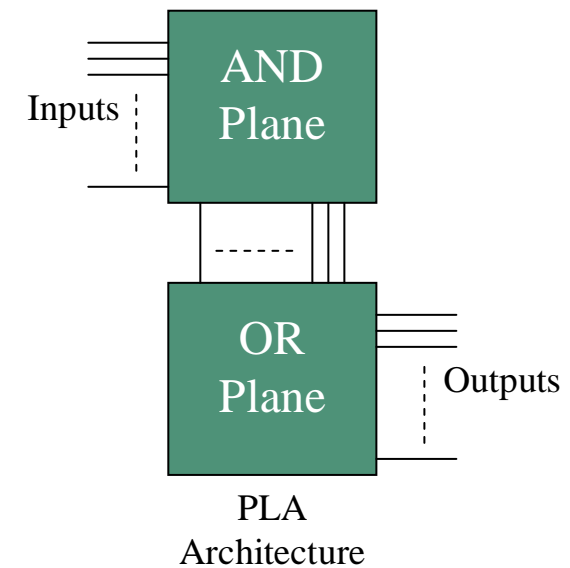
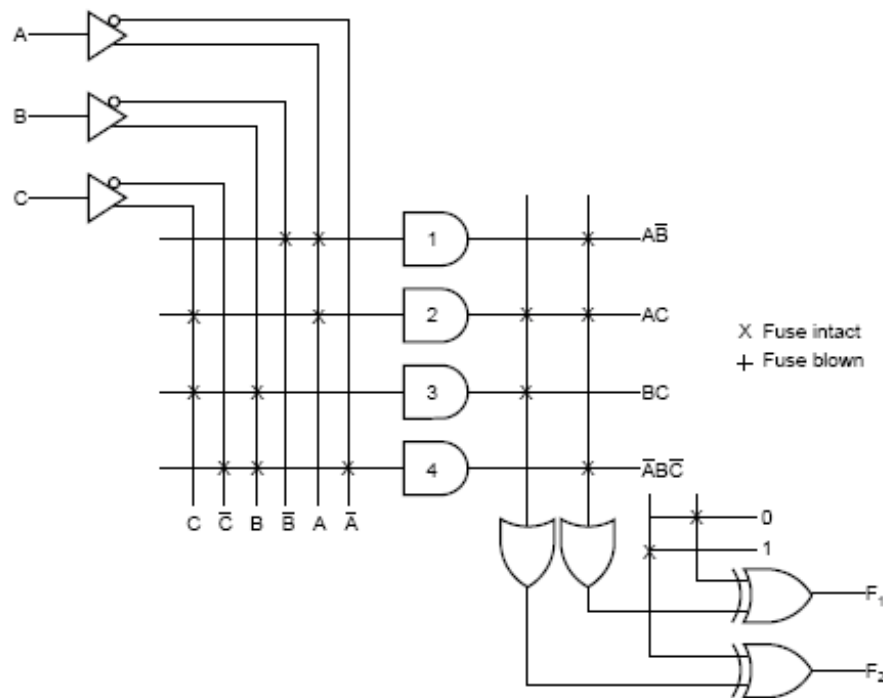
- ✓ First field programmable devices
- ✗ Slow access time
 - ↳ Not useful for applications where speed is an issue
- ✗ Limited number of inputs
- ✗ Require different technology
 - ↳ Extra masks
 - ↳ Extra processing steps
 - ↳ Extra development time
 - ↳ Extra cost



PLAs: Programmable Logic Arrays

- ❑ Classified as a simple programmable logic device (SPLD)
- ❑ The first programmable logic device introduced in the early 1970s by Philips.
- ❑ Based on the idea that logic functions can be realized in sum-of-products form.
- ❑ A programmable AND array followed by a programmable OR array.
- ❑ HDLs to convert Boolean equations into connections
 - ↳ ABEL
 - ↳ PALASM

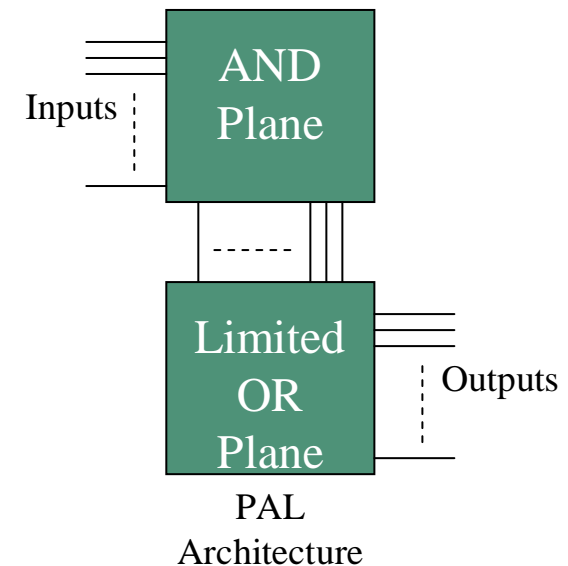
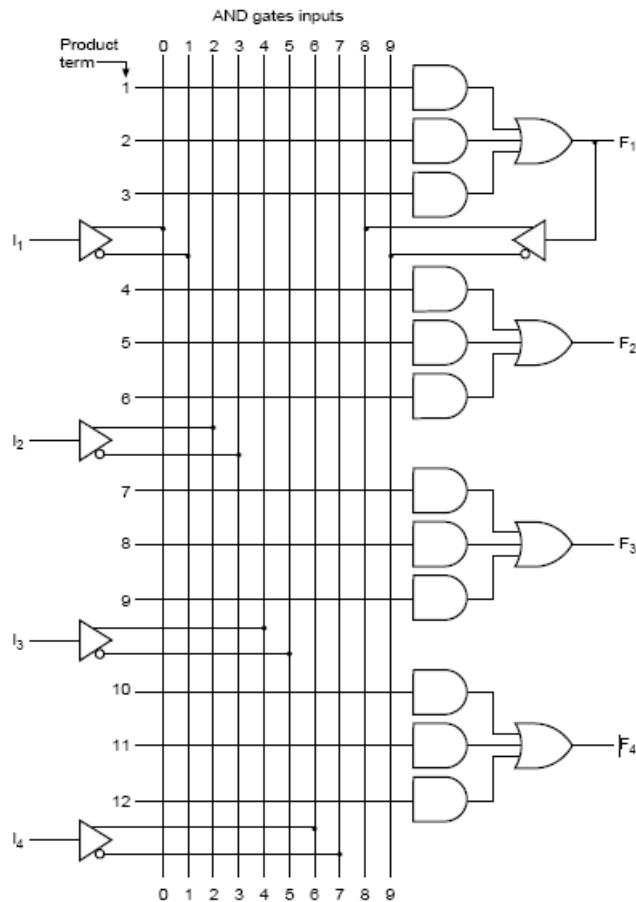
PLAs: Programmable Logic Arrays



PALs: Programmable Array Logic

- ❑ A device similar to PLA.
- ❑ Introduced to overcome the weaknesses of PLAs at that time (programmable switches were hard to fabricate correctly and introduced significant propagation delays).
- ❑ A programmable AND array followed by a fixed OR array. Inverters at the inputs and outputs.
- ❑ HDLs to convert Boolean equations into connections
 - ↪ ABEL
 - ↪ PALASM

PALs: Programmable Array Logic



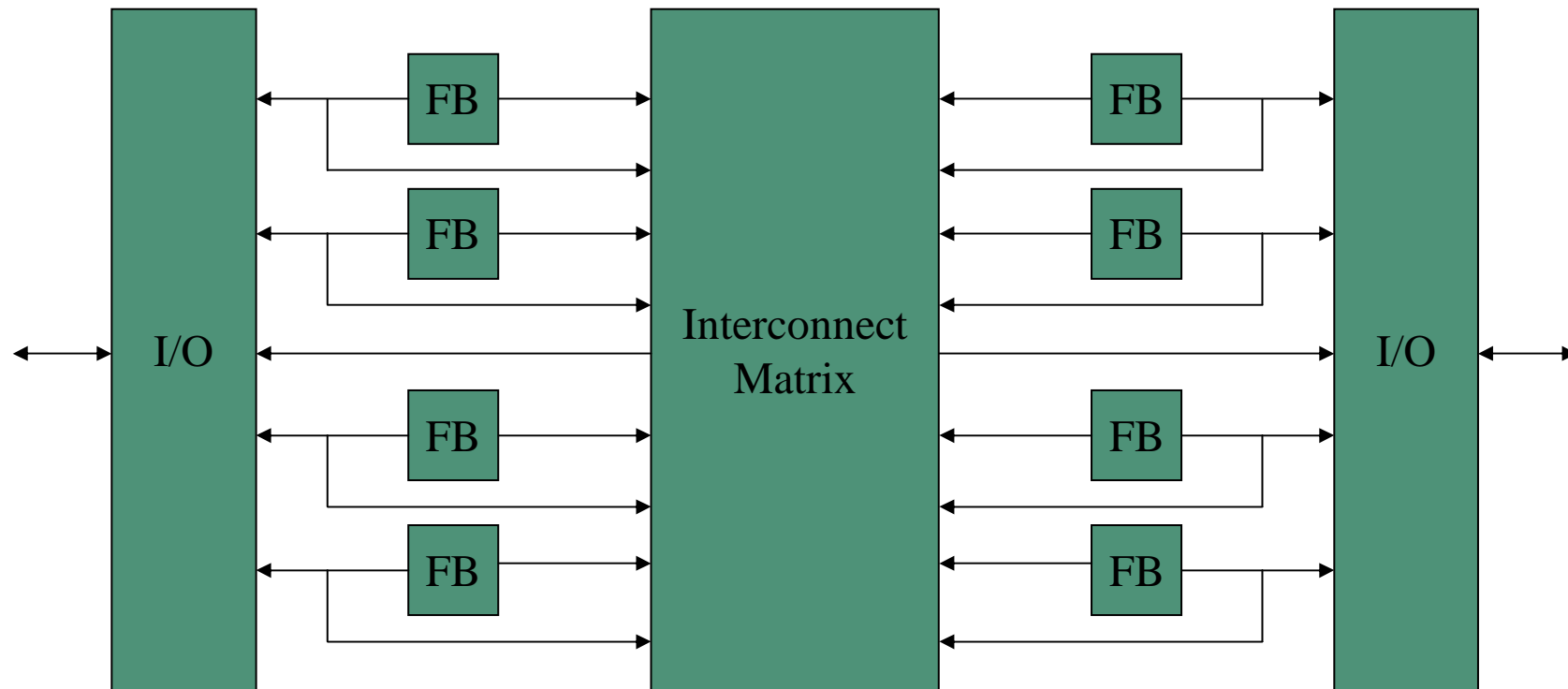
First idea of an FPGA/CPLD different from a PLD:

- 1984: Ross Freeman / Zilog, Inc.
 - ↳ Xilinx, Inc. with \$4.25M in venture capital

- 1983: Altera Corp.

- 1985: Actel Corp. with FPGAs based on antifuse switching elements

Large number of PALs in a single chip



CPLD Architecture (Altera)

Function Block

- ❑ Typically similar to a PAL architecture
- ❑ Same technology and programming tools than a PAL
- ❑ Additional specialized logic in each FB:
XOR (difficult in a PAL), Muxes, FFs...
- ❑ Additional embedded devices in the CPLD:
 - ↳ SRAM and Flash memories
 - ↳ Microcontrollers and microprocessors
 - ↳ Digital Signal Processors (DSPs)
 - ↳ Phased Locked Loops (PLLs)
 - ↳ Network processors

Selection criteria

- ❑ The programming technology
 - ↳ Equipment for device programming
- ❑ The FB capability
 - ↳ #FFs, #inputs, built-in XORs ...
- ❑ The number of FB in the device
- ❑ The kind of FF control available
- ❑ Embedded devices
- ❑ The number and type of IO pins
- ❑ The number of clock input pins

Field

Programmable

Gate

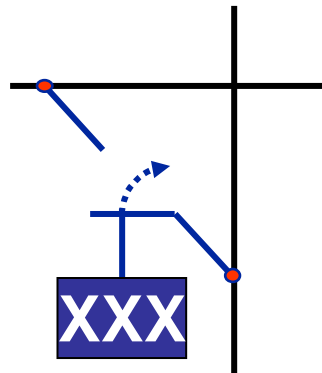
Array

A large number of logic gates in an IC array that can be connected (configured) electrically

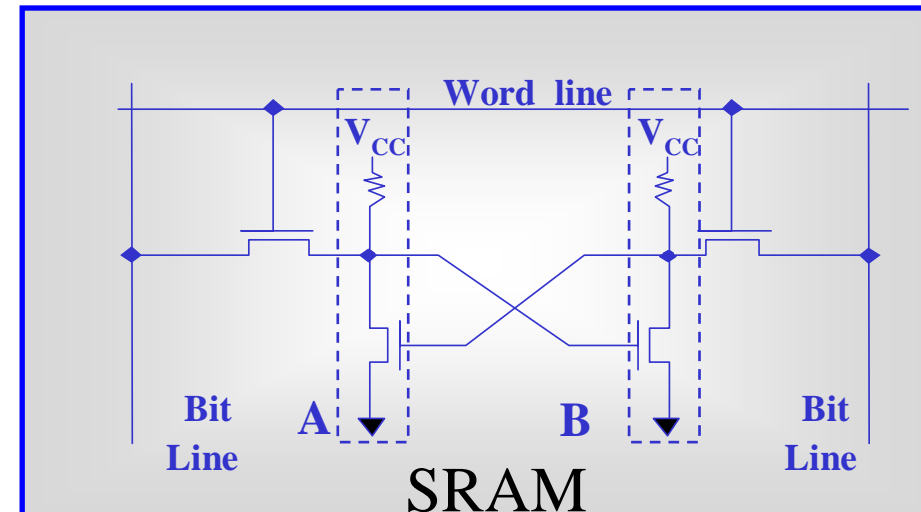
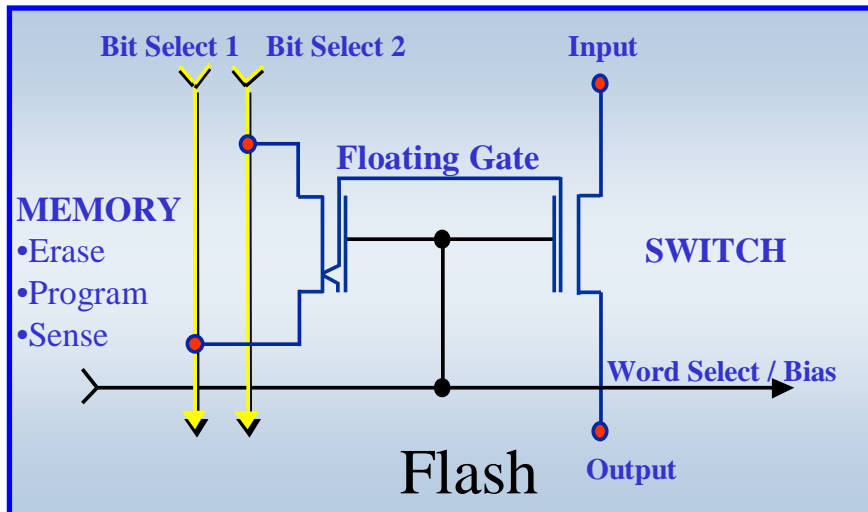
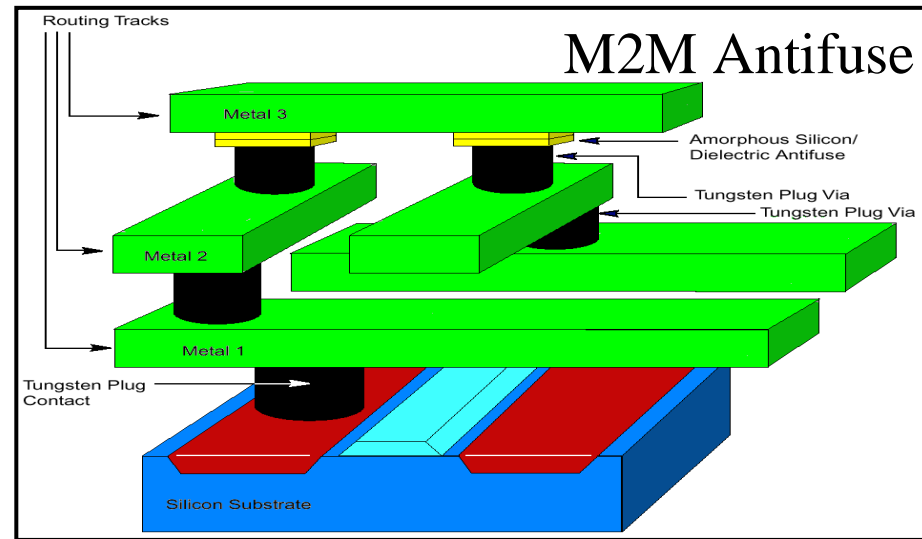
▪ **The Four Components of FPGAs**

- **The Configuration Element**
- **The Logic Module**
- **The Memory**
- **Control Circuits/Special Features**

■ The Interconnect Switch



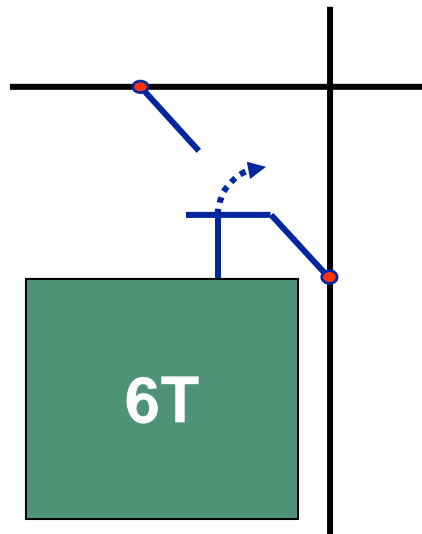
FPGA Industry Interconnect (Switch) Technologies



FPGA Technologies Compared



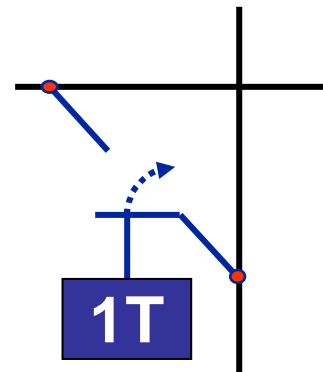
SRAM



Reprogrammable

Large Switch
expensive wires
Low Logic Utilization
typ 60%

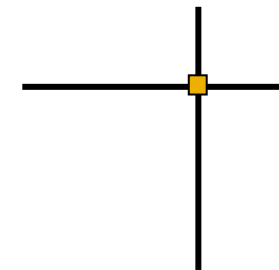
Flash



Best of Both Worlds
Reprogrammable
& Nonvolatile

Small Switch
cheap wires
High Logic Utilization
typ >85%

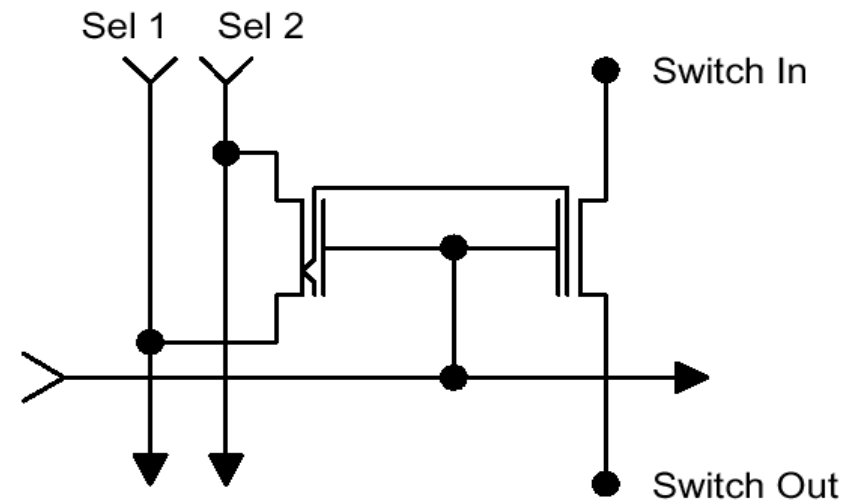
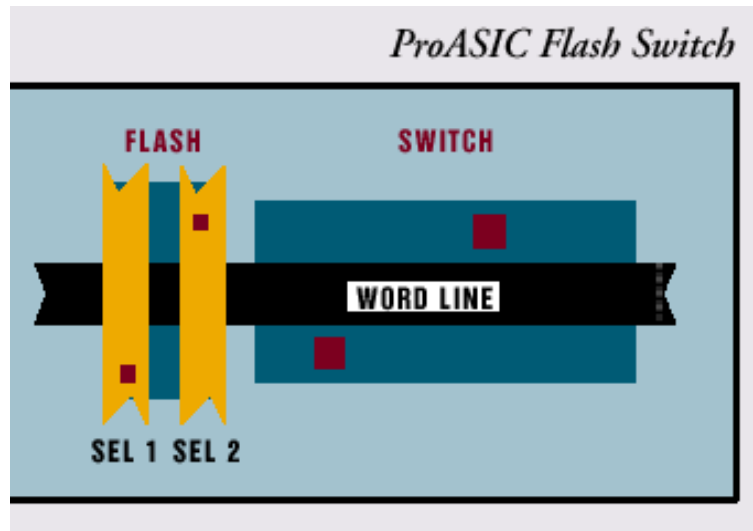
Anti-fuse



Nonvolatile

Smallest Switch
cheapest wires
Highest Logic Utilization
typ >90%

ProASIC, ProASIC^{Plus}, ProASIC III Routing Switch

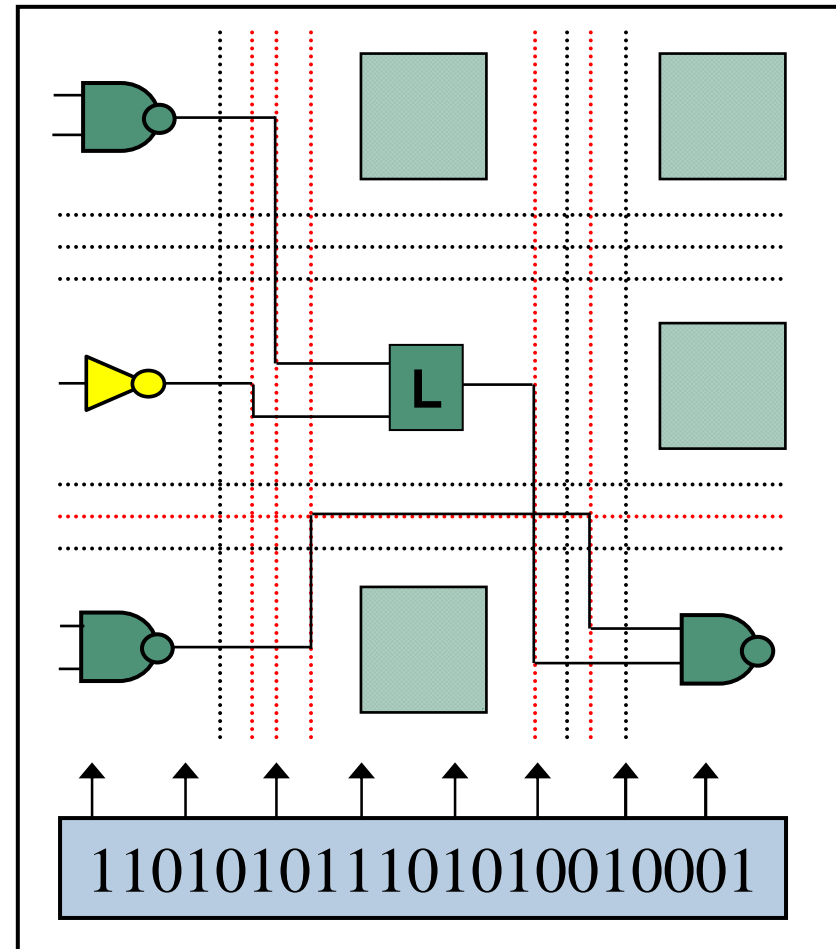
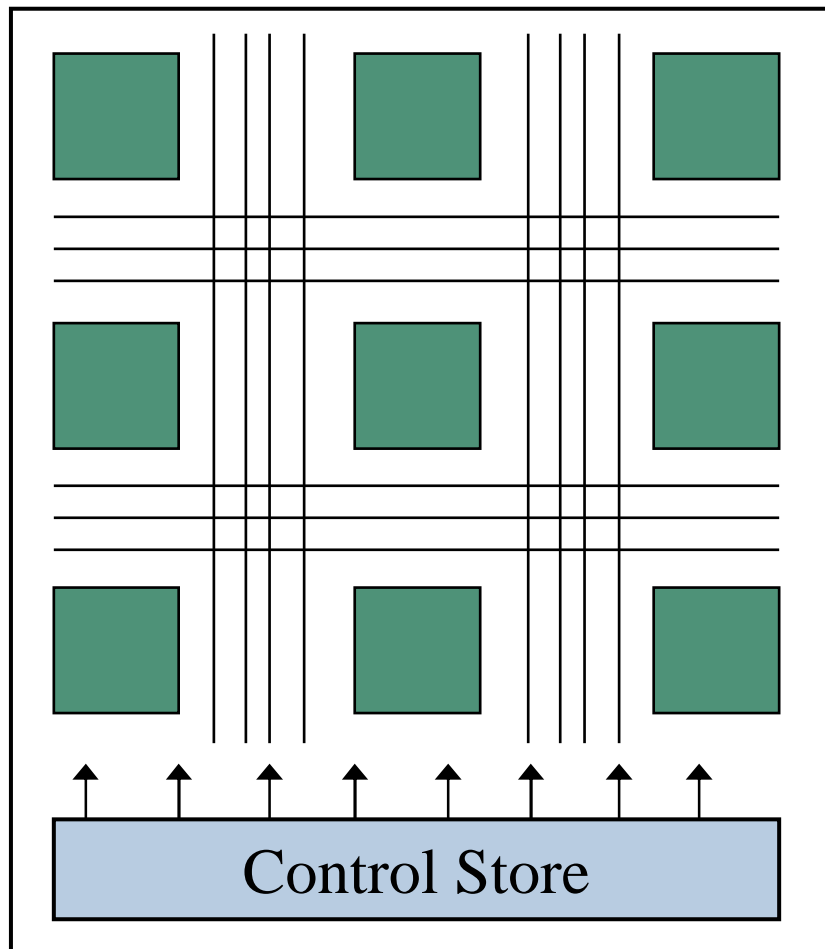


- Volatile (loses its configuration when power is turned off)
 - **Reprogrammable: SRAM** process and device technology
 - ◆ Xilinx, Altera, Lattice

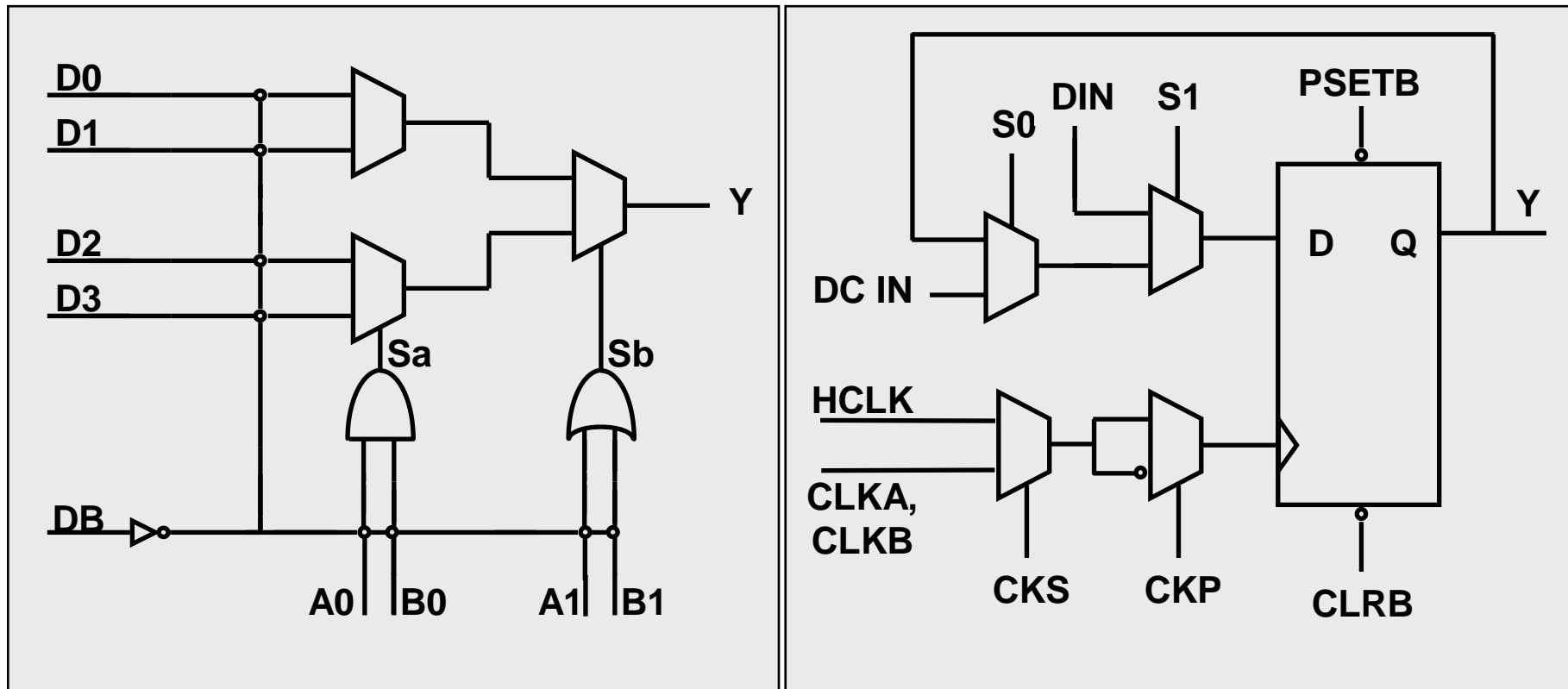
- Non-Volatile (keeps its configuration)
 - **One Time Programmable (OTP): Anti-fuse**
 - ◆ Actel, Quicklogic
 - **Reprogrammable: Flash**
 - ◆ Actel

Field Programmable Gate Arrays (FPGAs)

Regular array of logic



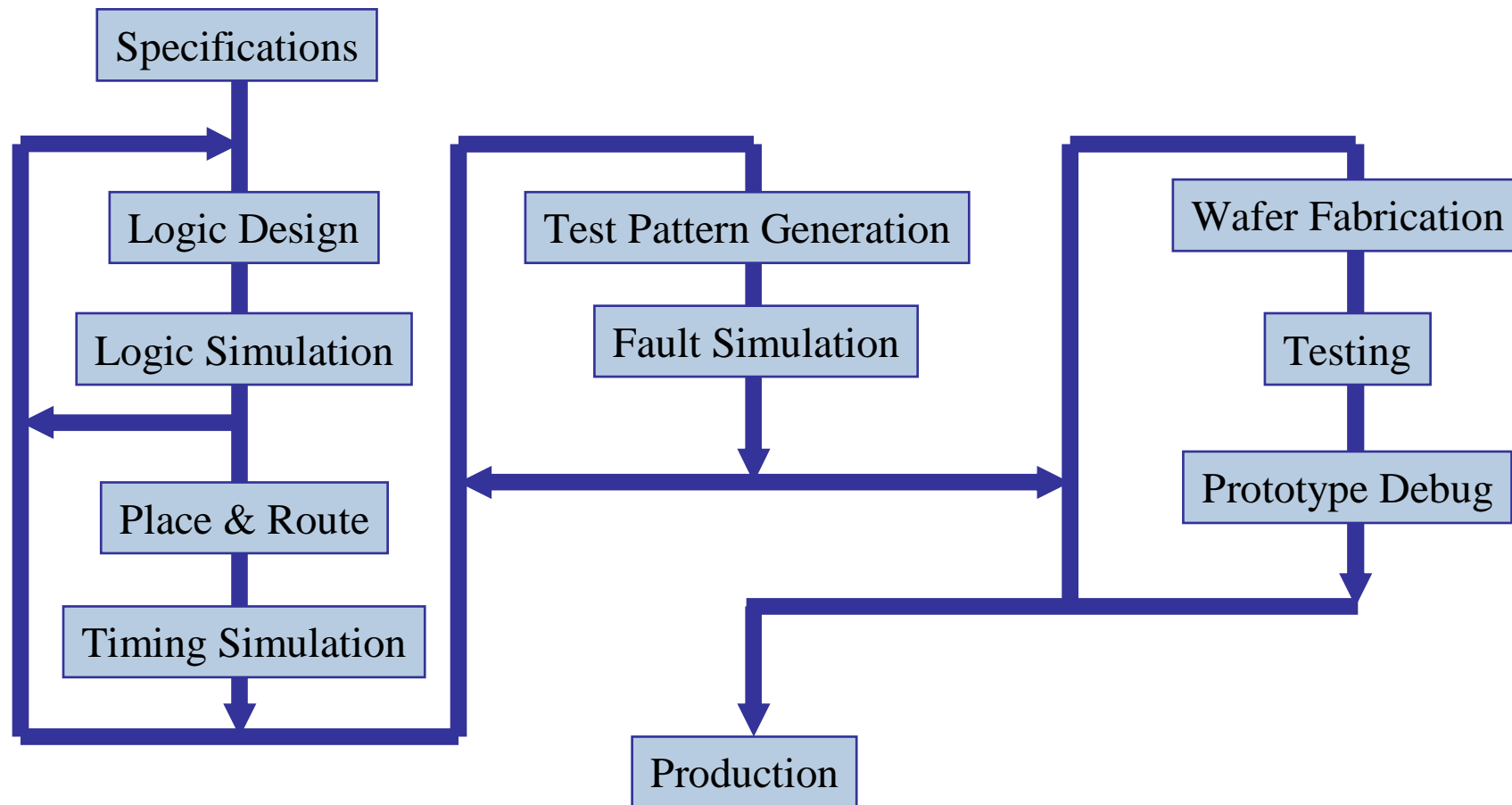
Configurable logic blocks

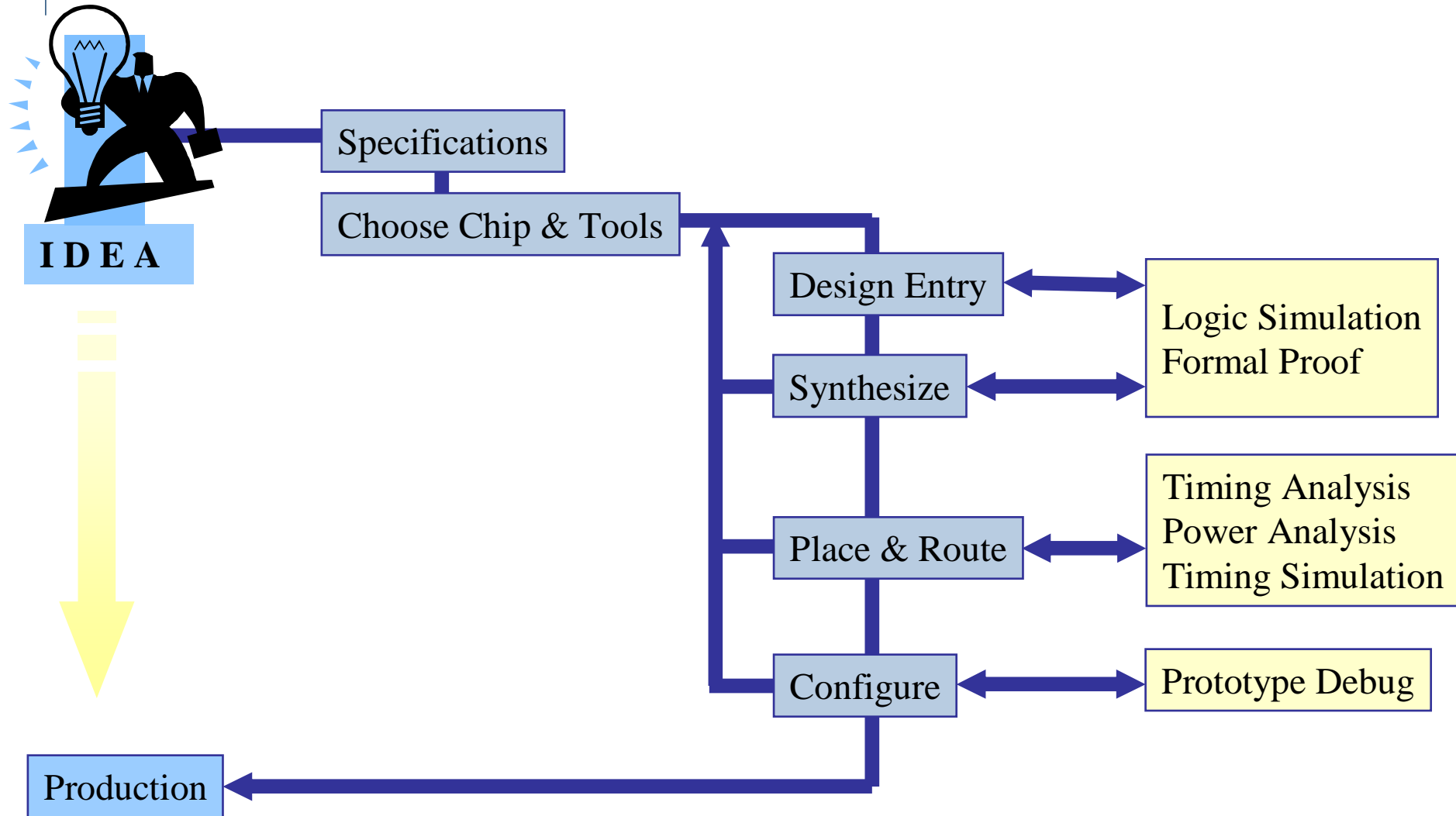


Selection criteria

- ❑ Programming technology
- ❑ Configurable logic block
 - ↳ #FFs, #inputs, ...
- ❑ The number of logic blocks in the device
- ❑ Embedded devices
- ❑ The number and type of IO pins
- ❑ The number of clock input pins

	CPLD	FPGA
Architecture	PAL-like	Gate array like
Speed	Fast, predictable	Application dependent
Density	Low to medium	Medium to high
Interconnect	Crossbar	Routing
Power consumption	High per gate	Low per gate





Specifications

- ❑ External block diagram (chip in the system)
- ❑ Internal block diagram
- ❑ Description of the IO pins
- ❑ Timing & power constraints
 - ↳ Clock frequency, external setup, external hold, ...
- ❑ Gate count estimate
- ❑ Package type
- ❑ Price target
- ❑ Test procedure

Choosing Device and Tools

- Synthesis
 - ↳ Coding style for the HDL

- ...

Design

- ❑ Partitioning ⇒ Implementation ⇒ Assemblage
- ❑ Top-down flow
- ❑ Work with the device architecture
- ❑ Do synchronous design
- ❑ Protect against metastability
- ❑ Avoid floating nodes
- ❑ **VERIFY AT EACH STEP**

Verification

- ❑ Simulation
- ❑ Design review
- ❑ Timing analysis
- ❑ Power analysis
- ❑ Formal verification