The Abdus Salam
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Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

26 October - 20 November, 2009

VHDL & FPGA Architectures
Design Verification & Timing Concepts

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VHDL & FPGA Architectures

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Outline

- Introduction to FPGA & FPGA Design Flow
- Synthesis I – Introduction
- Synthesis II - Introduction to VHDL
- Synthesis III - Advanced VHDL
- Design verification & timing concepts
- Programmable logic & FPGA architectures
- Actel ProASIC3 FPGA architecture

Design Verification and Timing Concepts

Timing in the Design Flow

- Timing Driven Synthesis
- Timing Driven Optimization
- Timing Driven Floor-Planner
- Timing Driven Place & Route

Simulators versus Verifiers

- Simulators
  - **Circuit-Level**
  - **Timing**
  - **Switch-Level**
  - **Logic-Level**

- Verifiers (Pattern Independent)
  - **Static Timing Analysis**

Timing Driven Methodology

- Barto's Law:

Every circuit is considered guilty until proven innocent

- Golden Rule:

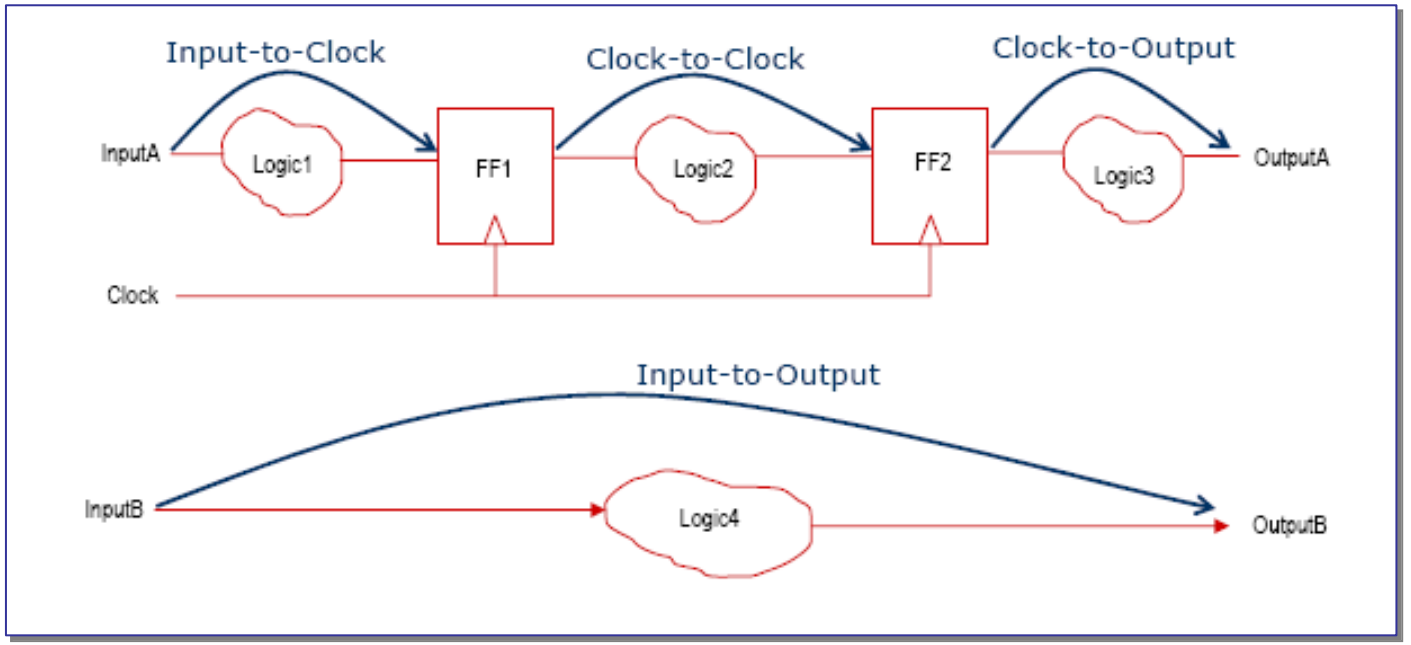
Detect Problems as early as possible

What are Timing Constraints?

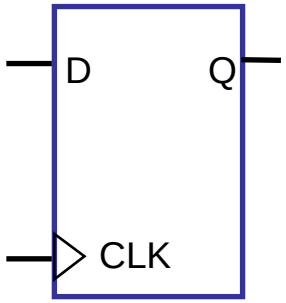
- Maximum or minimum limits placed on timing paths
- Usually expressed in ns. or ps.
- There are basically 4 types of timing paths in a synthesized digital design:
  - **Input to registers**
  - **Registers to output**
  - **Input to output**
  - **Registers to registers**
- To understand timing paths we first must understand flip-flop timing parameters

Timing Paths

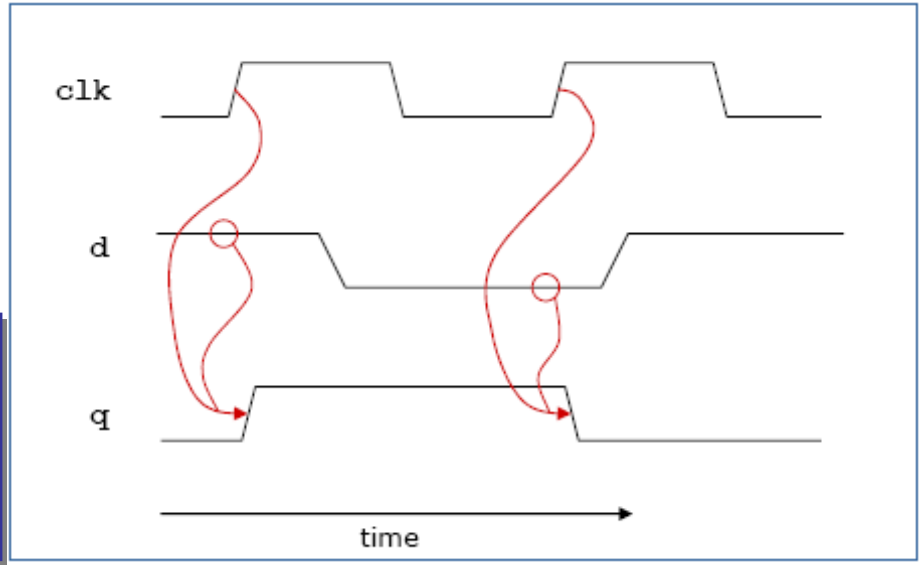
- These basic timing paths can apply to:
  - **A module within an ASIC/FPGA**
  - **A whole ASIC/FPGA**
  - **A system with multiple chips**



Flip-Flop Timing

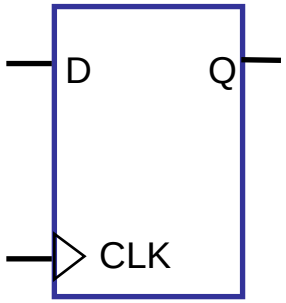


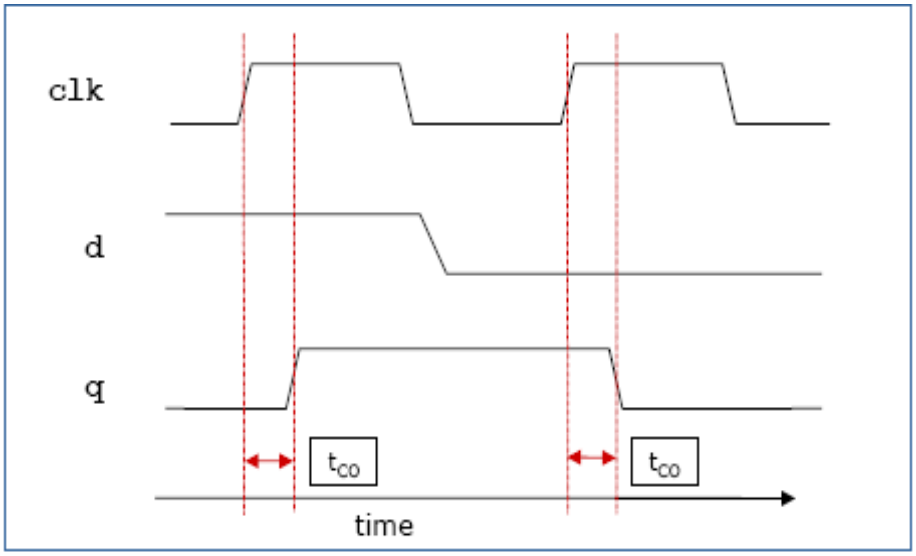

```
INFER: process (CLK) begin
  if (CLK'event and CLK ='1') then
       Q  <= D;
  end if ;
end process INFER;
```



- The level of d is sampled on the rising edge of clk
- q holds the sampled value until the next clk rising edge
- The level of d must be stable for some amount of time before and after the sampling clock edge

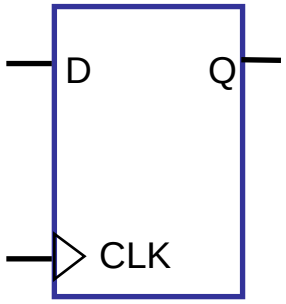
Flip-Flop Timing Parameters

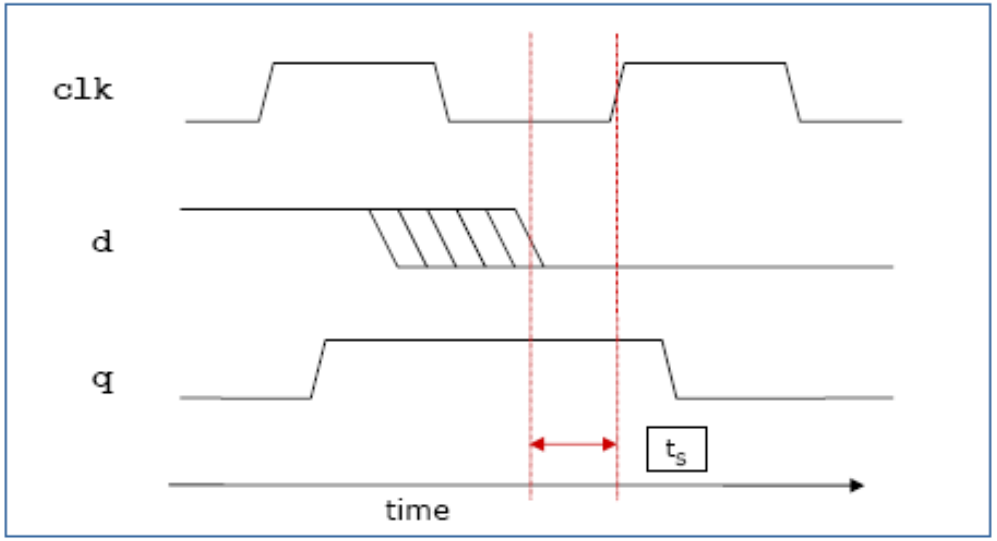




- Clock-to-out (t_{CO}) a.k.a. Clock-to-Q
  - **The time delay from the active edge of the flip-flop's clock input to the resulting change in the Q output**
- Specified minimum and maximum times

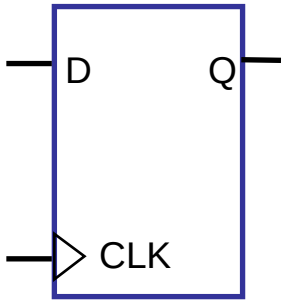
Flip-Flop Timing Parameters (cont'd)

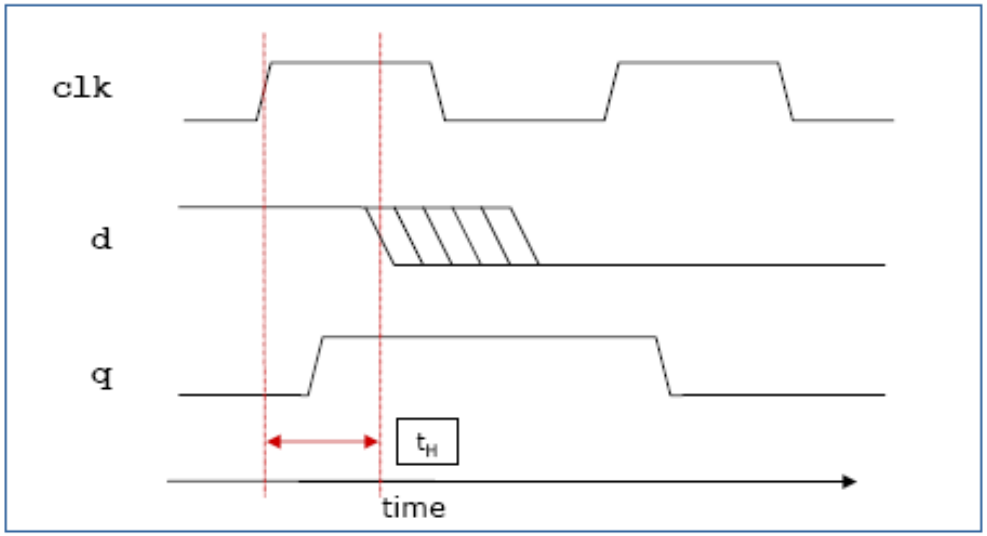




- Input Setup (t_S)
  - **The minimum time that the D input must be stable before the active (rising or falling) edge of the clock**

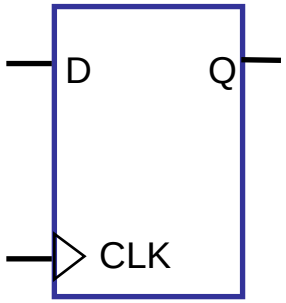
Flip-Flop Timing Parameters (cont'd)

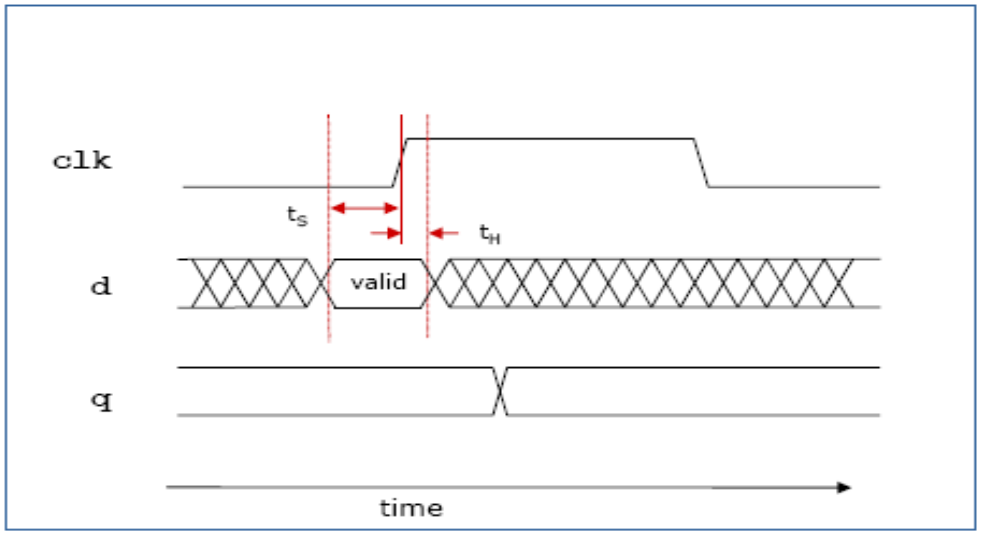




- Input Hold (t_H)
  - **The minimum time that the D input must be stable after the active edge of the clock**

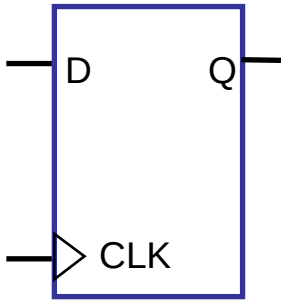
Flip-Flop Timing Parameters (cont'd)

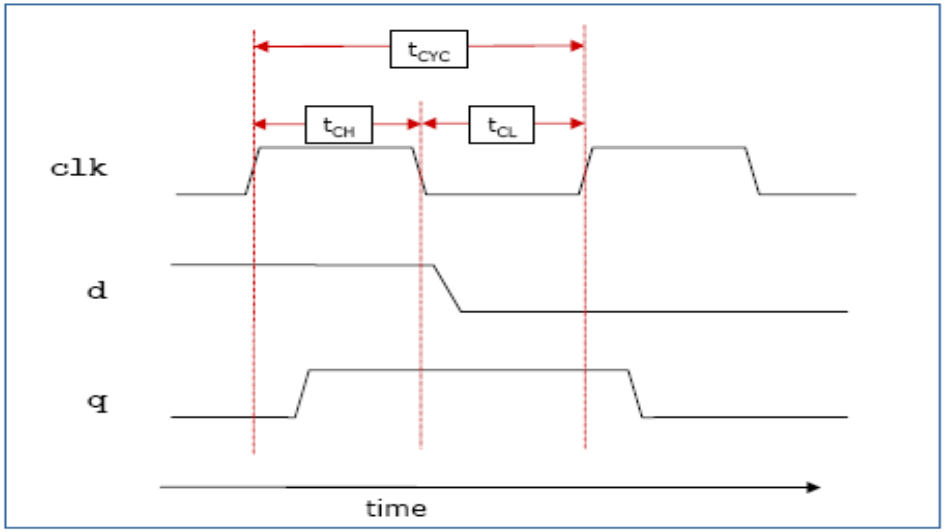




- Setup and Hold define a minimum window around the active clock edge during which D must be stable
- t_S or t_H may be negative, but $t_S + t_H > 0$

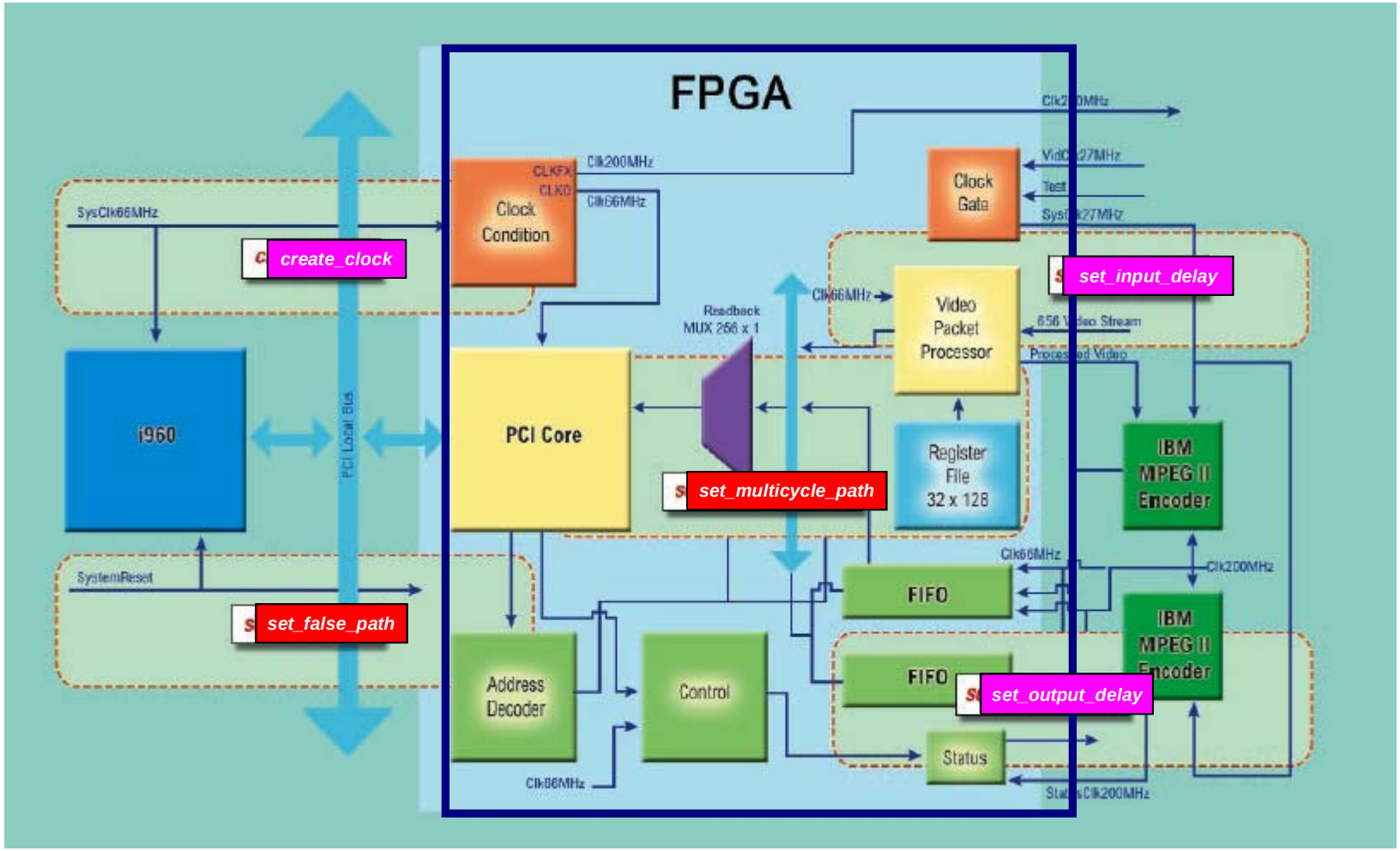
Flip-Flop Timing Parameters (cont'd)





- Clock Parameters
  - **Clock cycle time (t_{CYC}), minimum**
  - **Clock pulse width high (t_{CH}), minimum**
  - **Clock pulse width low (t_{CL}), minimum**

Constraining FPGA Designs with SDC



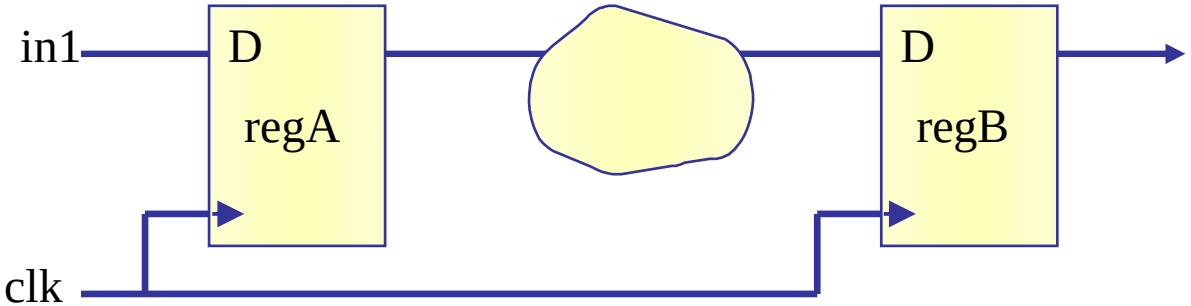
Source: Mentor Graphics Corporation ©, 2002

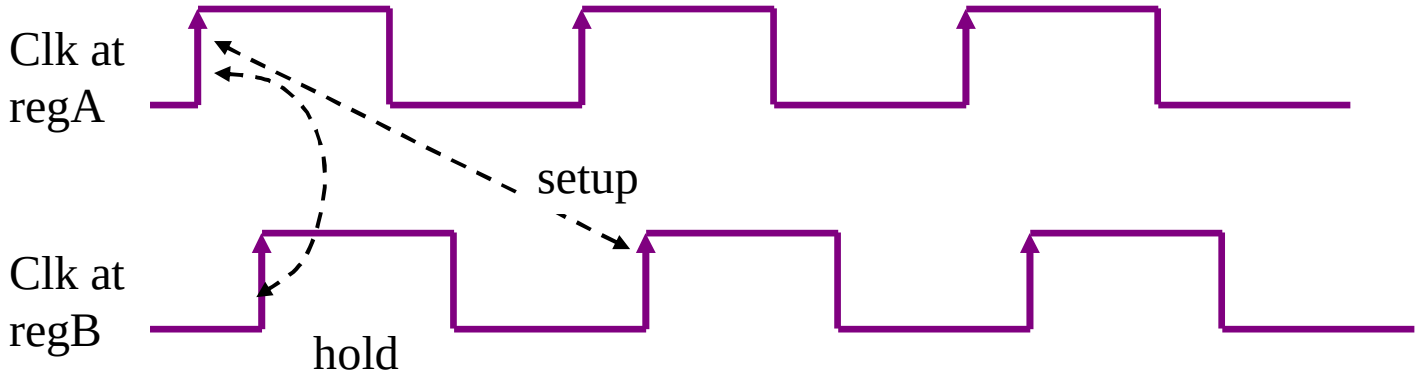
Constraining Designs

- Design Environment
  - **Operating conditions (Process / Voltage / Temperature)**
    - **Worst: to fix the setup violations**
    - **Typical: mostly ignored**
    - **Best: to fix the hold violations**
- Timing Assertions (Design-level)
  - **Clock Characteristics**
  - **Arrival Time at Each Input Port**
  - **Required Time at Each Output Port**
- Timing Exceptions
  - **False Paths**
  - **Maximum Path Delay**
  - **Minimum Path Delay**
  - **Multi-cycle Paths**

Timing Analysis: Setup/Hold Check

- Create Clock: reg-to-reg requirement

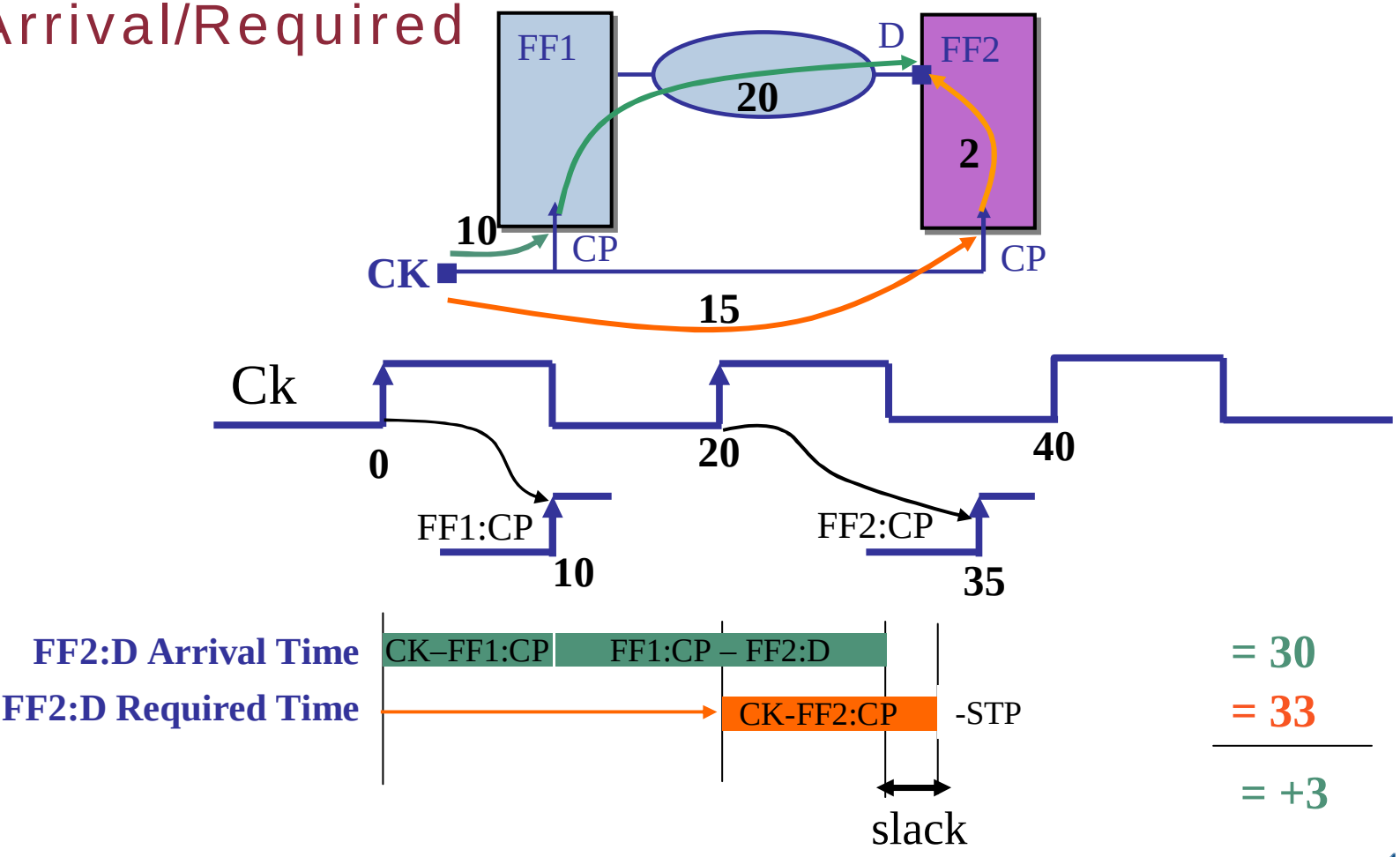




Single-cycle timing relationship

Setup Check

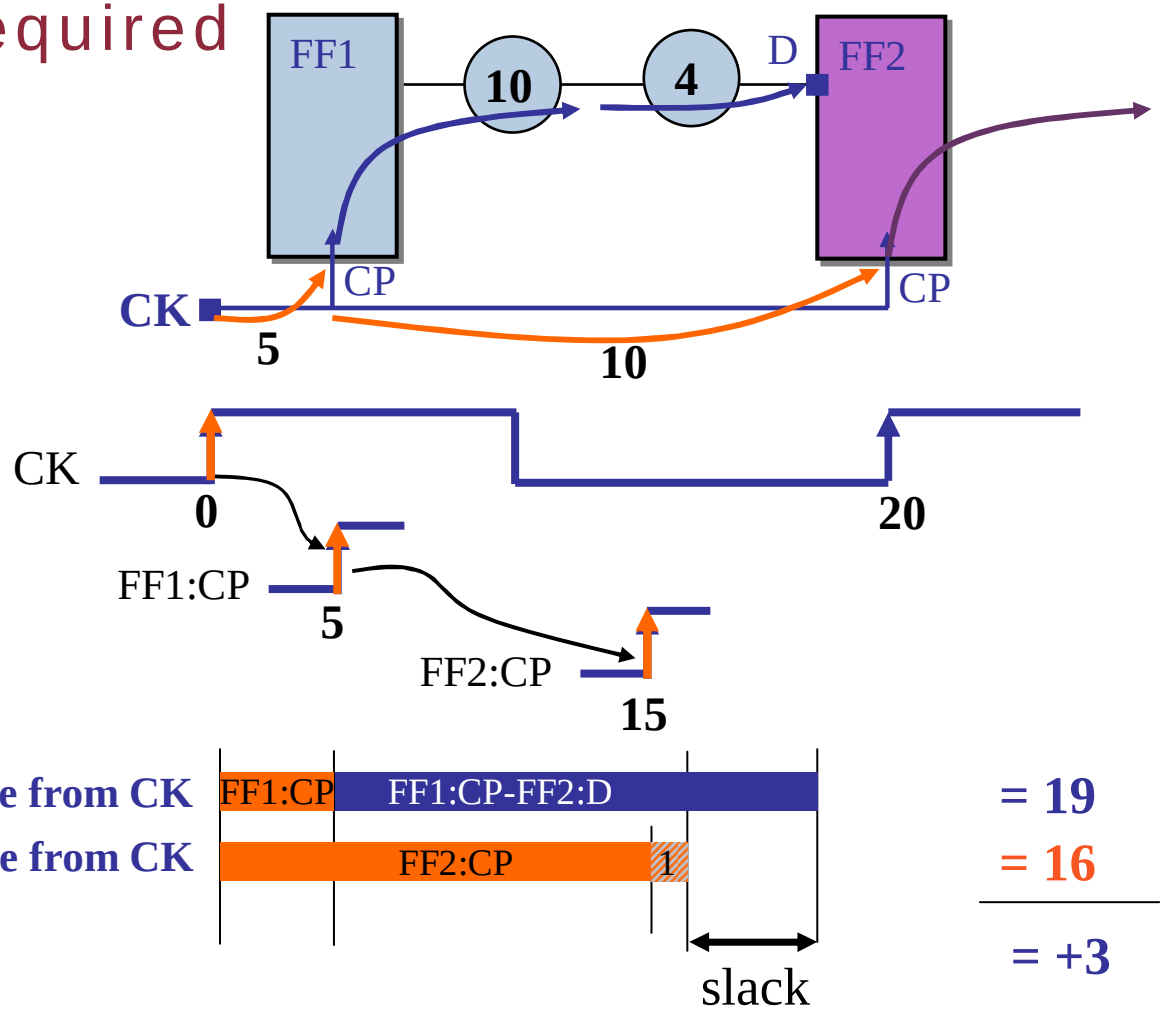
- Arrival/Required



Slack = Required_time – Arrival_time (Violation if < 0)

Hold Check

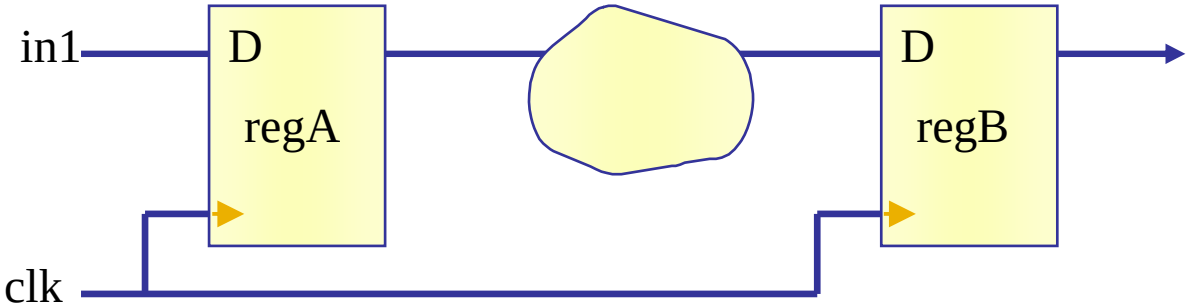
- Arrival/Required

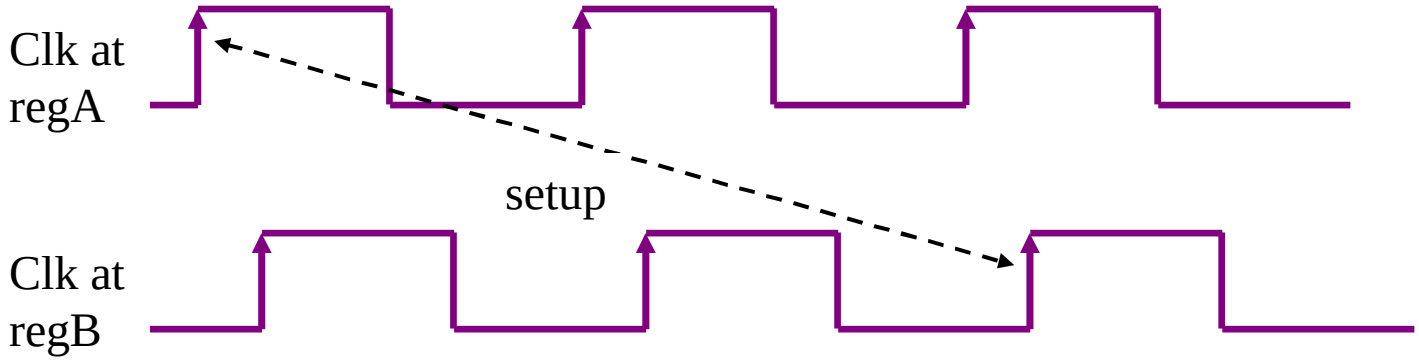


Slack = ArrivalTime – RequiredTime (Violation if < 0)

Timing Analysis: Multi-cycle

- set_multicycle_path: reg-to-reg exception

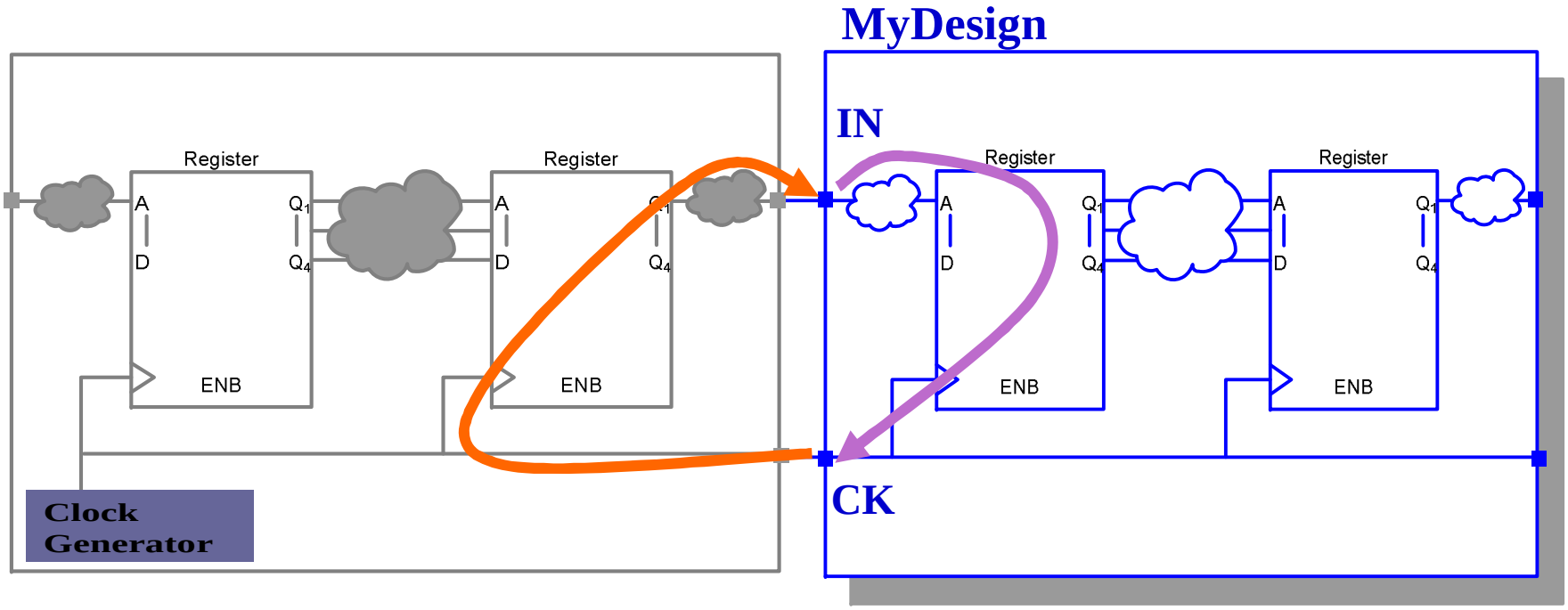


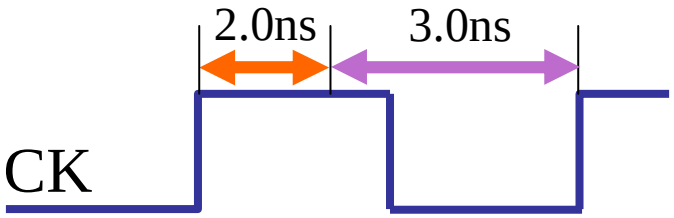


multi-cycle timing relationship

Input Delay Constraints

- Captures External Setup/Hold Requirements



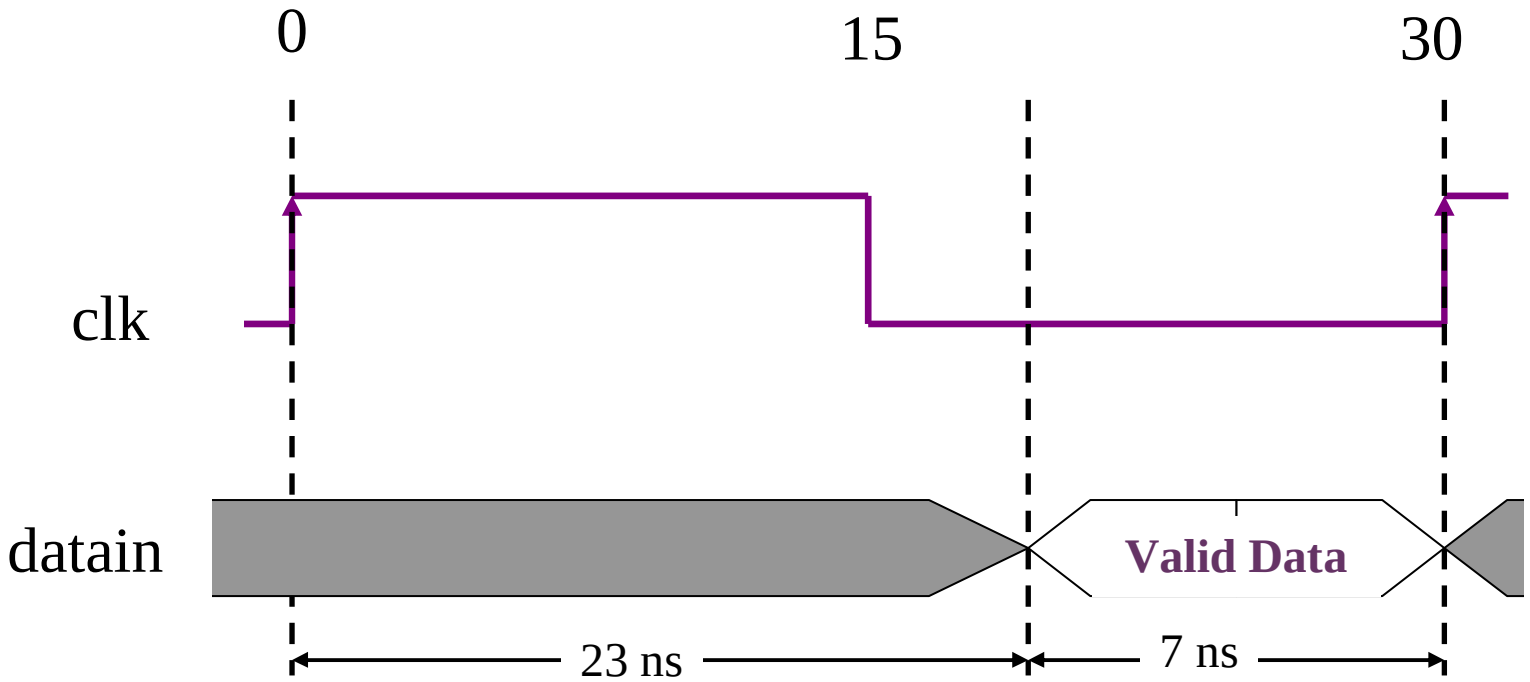


Option "-min" for hold check
Option "-max" for setup check

SDC: set_input_delay 2.0 -clock CK {IN}

Constraining Designs

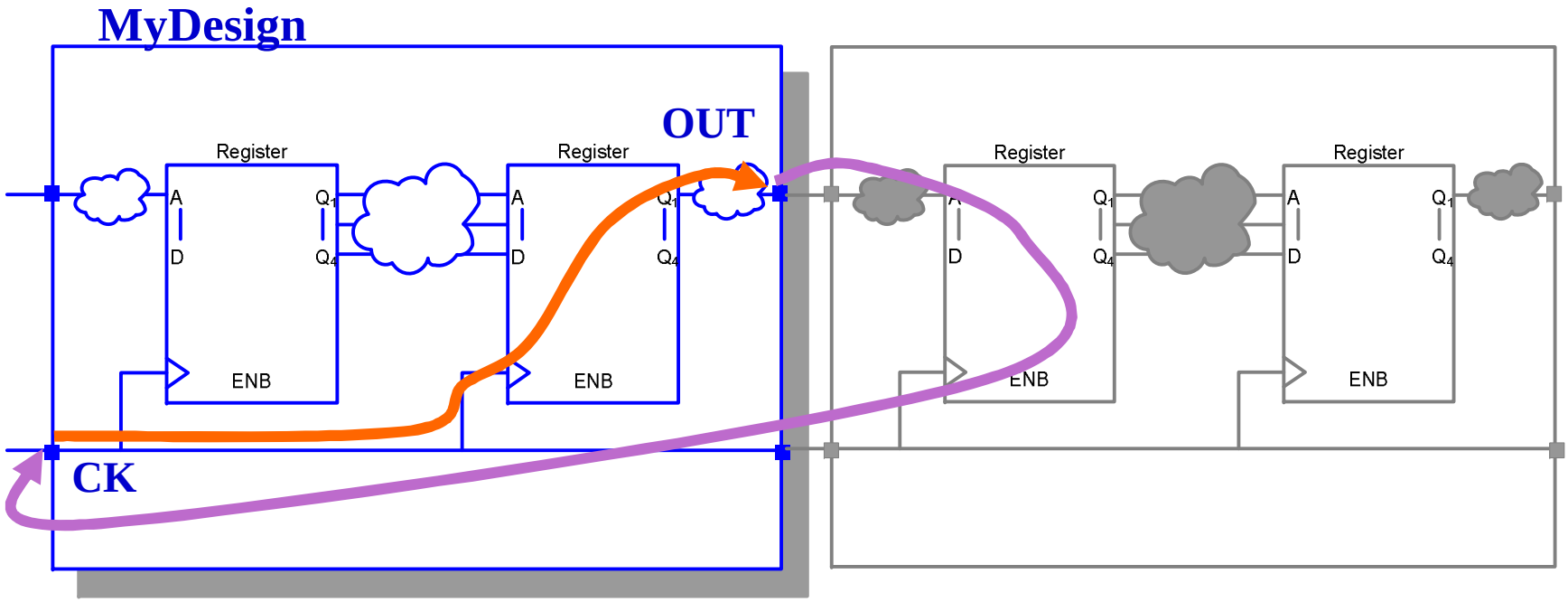
- Set Input Delay: setup/hold requirements

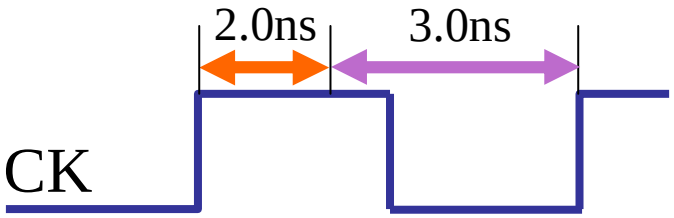


> set_input_delay -max 23.0 -min 0.0 -clock clk {datain}

Output Delay Constraint

- Captures Clock-to-Out Requirements



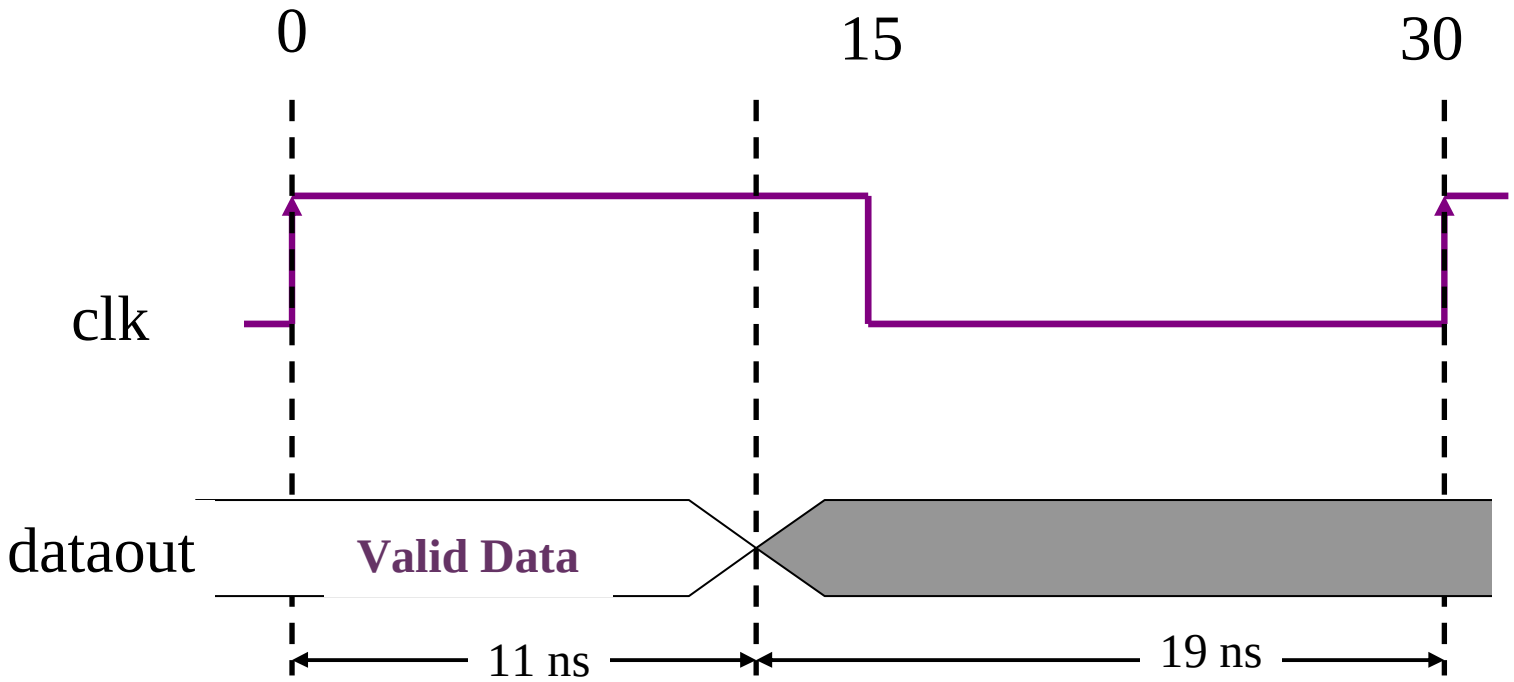


Option "-min" for hold check
Option "-max" for setup check

SDC: set_output_delay 3.0 -clock CK {OUT}

Constraining Designs

- Set Output Delay: clock-to-out requirement

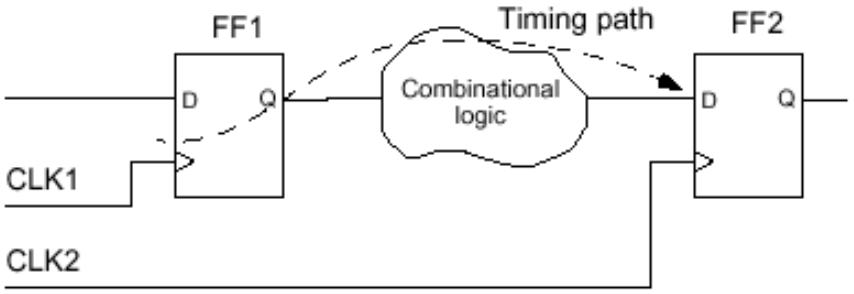


> set_output_delay -max 19.0 -clock clk {dataout}

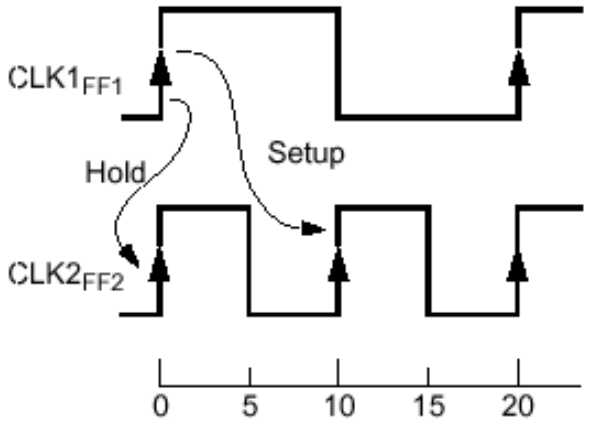
Cross-Domain Analysis

- Study over the Least Common Multiplier

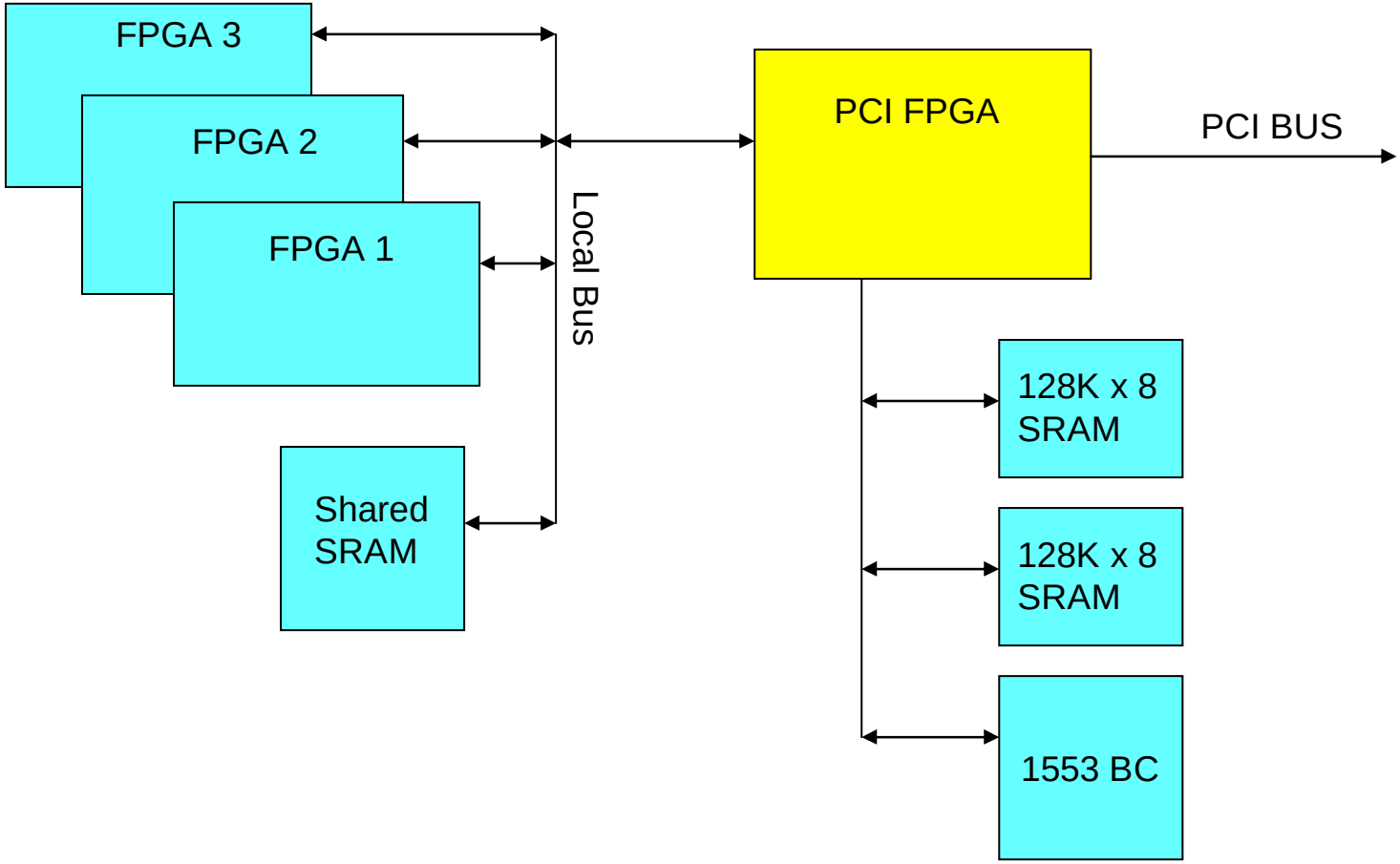
common period




```
pt_shell> create_clock -period 20 -waveform {0 10} CLK1
pt_shell> create_clock -period 10 -waveform {0 5} CLK2
```

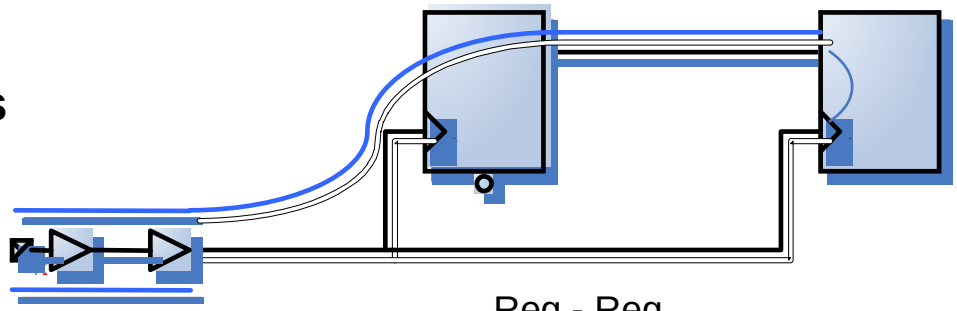


Design Overview
Block Diagram

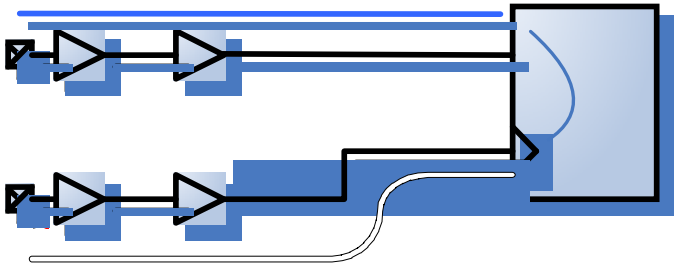


Design Overview
System Timing Requirements

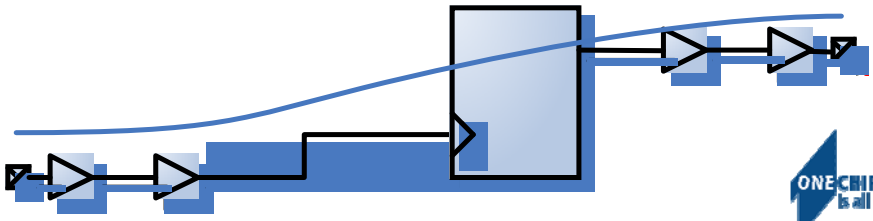
- PCI
  - **33 MHz Clock**
  - **External set up time – 7 ns**
  - **Clock to output – 10 ns**
- Local Bus
  - **24 MHz Clock**
  - **I/O is asynchronous**



Reg - Reg



External Setup



Clock to Out

Design Overview
Timing Closure Loop