



2065-21

Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

26 October - 20 November, 2009

Liberto TM Integrated Design Environment

Nizar Abdallah ACTEL Corp. 2061 Stierlin Court Mountain View CA 94043-4655 U.S.A.



Libero[™] Integrated Design Environment



Agenda

- Libero Overview
- 3rd Party Tools
- Designer Overview
- Programming
- Silicon Explorer
- Reference Material



Libero IDE: A Complete FPGA Design Solution



Comprehensive Development Environment

- Design, implementation, validation, debug
- Supports full suite of Actel's power efficient FPGAs

Best in Industry Tools

- Industry leading synthesis and simulation tools
- High performance timing and power driven place & route
- SmartTime timing and bottleneck analysis speeds timing closure
- Accurate hierarchical power analysis with SmartPower

Relentless Pursuit of Ease of Design

- Push button flows hide design complexity
- GUI wizards guide design process
- Rich IP library & user block support facilitates design reuse



Libero IDE Gold Edition

World Class Fully-Integrated PC Development System

- Targets All Devices up to 1.5M Gates
- Tools:
 - ViewDraw AE v8.5
 - WaveFormer Lite 12.30a
 - ModelSim AE 6.4a
 - Synplify AE 9.4A (1.5M gates) SYNPLIFY-PRO
 - Actel Designer 8.5(1.5M gates)
 - FlashPro 8.5
 - Silicon Explorer 5.2
- PC Platform
 - Licensed to Disk ID (Node-Locked license)
- 1 Year Free License!
 - No Updates (Service Packs Available)

Tool Features

Integrated Design Management	>
Schematic	>
VHDL	>
Verilog	>
Macro Generation	<
Testbench Generator	<
VHDL Simulation Verilog Simulation	~
Timing Simulation	~
Static Timing Analysis	>
Timing Driven Place and Route	<
Push Button Place and Route	<
Layout Editor	~
Silicon Explorer	~
Standard Industry Interfaces	~
Third Party Design Libraries	~

SP2	~
Win Vista	
Business	~



Libero IDE Platinum Edition

Windows Support

World Class Fully Integrated PC Development System

- Targets All Actel Devices
- Tools
 - ViewDraw AE v8.5
 - WFL 12.30a with Reactive Testbench Generation
 - ModelSim AE 6.4a
 - Synplify Pro AE 9.4A (*No* Gate Limit)
 - Actel Designer 8.5 (No Gate Limit)
 - FlashPro 8.5
 - Silicon Explorer 5.2
- License Types
 - Node-Locked License Tied to Disk-id or Hardware Keys
 - Floating License
- Price:
 - \$2495 First Year / \$1995 Renewal
 - Free 45 day Evaluation License

Tool Features

Integrated Design Management	<
Schematic	<
VHDL	<
Verilog	•
Macro Generation	<
Testbench Generator	<
VHDL Simulation Verilog Simulation	>
Timing Simulation	<
Static Timing Analysis	<
Timing Driven Place and Route	<
Push Button Place and Route	<
Layout Editor	•
Silicon Explorer	~
Standard Industry Interfaces	>
Third Party Design Libraries	>

WinXP Pro	
SP2	\checkmark
Win Vista	
Business	~



Libero IDE Solaris and Linux Support

- Libero Solaris, Libero Linux
 - Tools
 - Project Manager
 - Synplify Pro AE
 - ModelSim AE VHDL & Verilog
 - Designer
 - Supports All Devices
 - License Type: Floating
 - Solaris: Host ID only
 - Linux: requires USB key for Synplify
 - 1 Year License: \$2495
 - Renewal: \$1995
 - Free 45 day Evaluation License



Libero IDE Edition Summary

		Libero Platinum	Libero Platinum	Libero Platinum
	Libero Gold	(Windows)	(Solaris / Linux)	Eval
	All devices up			
Device Support	to 1.5M Gates	All Devices	All Devices	All Devices
ViewDraw	AE	AE	-	AE
		Reactive		
WaveFormer Lite	AE	Testbench	-	Reactive Testbench
Synthesis	Synplify AE	Synplify Pro AE	Synplify Pro AE	Synplify Pro AE
ModelSim	AE	AE	AE	AE
Designer	Yes	Yes	Yes	Yes
FlashPro	Yes	Yes	-	No
Explorer	Yes	Yes	-	No
				Disk ID (Windows)
				Floating (Solaris /
License Type	Disk ID	Key or Disk ID	Floating	Linux)
Price	Free	\$2,495	\$2,495	Free 45 day



Libero IDE v8.5 Device Support by Edition

Family	Gold	Platinum and Eval
ACT1	1010B, 1020B, 10∨10B, 10∨20B	
ACT2/ACT3	1225A, 1240A, 1280A, 415A, 1425A, 1440A, 1460A, 14100A	
1200XL	1225XL, 1240XL, 1280XL	
DX	3265DX, 32100DX, 32140DX, 32200DX, 32300DX	
MX	40MX02, 40MX04, 42MX09, 42MX16, 42MX24, 42MX36	
RH	RH1020, RH1280	
RT	RT1020, RT1425A, RT1280A, RT1460A, RT14100A, RTSX32SU, RT54SX72SU, RTAX250S, RTAX1000S	RTAX2000S, RTAX4000S
RTAX-DSP		RTAX2000D, RTAX4000D
SX / SX-A	SX08, SX16, SX16P, SX32, SX08A, SX16A, SX32A, SX72A	
еХ	eX64, eX128, eX256	
Axcelerator	AX125, AX250, AX500, AX1000	AX2000
ProASIC ^{PLUS}	APA075, APA150, APA300, APA450, APA600, APA750, APA1000	
	A3P015, A3P030, A3P060, A3P125, A3P250, A3P400, A3P600,	
ProASIC3	A3P1000, A3PE600, A3PE1500	A3PE3000
M7 / M1 ProASIC3	M7A3P1000, M1A3P250, M1A3P600, M1A3P1000, M1A3PE1500	M1A3PE3000
ProASIC3L	A3P250L, A3P600L, A3P1000L	A3PE3000L
ProASIC3 nano	A3PN030	
	AGL015, AGL030, AGL060, AGL125, AGL250, AGL600, AGL1000,	
IGLOO (1.2V / 1.5V)	AGLE600	AGLE3000
IGLOO PLUS	AGLP030, AGLP060, AGLP125	
M1 IGLOO (1.2V / 1.5 V)	M1AGL250, M1AGL600, M1AGL1000	
IGLOO nano (1.2V / 1.5V)	AGLN030	
Fusion	AFS090, AFS250, AFS600, AFS1500	
M7 / M1 Fusion	M7AFS600, M1AFS250, M1AFS600, M1AFS1500	

Libero IDE Installation

Libero IDE Project Manager

Libero IDE Design Explorer Window

- Hierarchy Tab Displays Hierarchical Representation of Source Files and Components in Project
 - Libero Automatically Updates Design Hierarchy





Libero IDE Design Explorer Window

- Files Tab Displays All Files in Project Grouped by Type
 - Components and user created files are displayed separately
 - Sort components by name or by type





Libero IDE Catalog Window: IP Cores Tab

- IP Based Design Flow
 - Access to a variety of IP Cores
- Configure and Instantiate Directly from Libero
 - No need to launch separate tools
 - No need to re-enter common information
 - No need to import generated cores
- Modify Generated Cores Directly from Libero
 - Change Configurations
 - Change Versions





Libero IDE Catalog Window: HDL Templates Tab

- VHDL and Verilog Templates
 - Facilitate the Writing of HDL Files by Inserting Predefined Language Constructs
 - Create User-defined Template
 Files





Libero IDE Project Manager: HDL Editor

Language-Sensitive HDL Editor

• Verilog 2001 or VHDL 93





Libero IDE Project Manager: Project Flow Window

- Tools Can Be Launched from Project Flow Window or Menus
- Step-by-Step Design flow Decreases Development Time
- Project Flow Window Displays:
 - Tools
 - Files
 - Transitions
 - Current State
 - Tool Tips
- Display Changes Dynamically Based on Target Family
- Tabs Switch Between Flow Window and HDL Window







Libero IDE Project Flow Window: File Status

- Group of Files Can Be ...
- ... Missing
 - If ANY Are Missing, Block Is Shadowed Out
- Available and Current
 - Green Check Mark Is Shown
- … Available, but Not Current 😃
 - If at Least One is Not Current, Warning Icon Is Displayed





Libero IDE Project Flow Window: Tool States

- Disabled => Button Is Shadowed
- White => Available, but Not Yet Used
- Green => Completed Successfully
- Red => Error in Running Tool





Libero IDE Project Flow Window: Config Options

 Project Flow Window Can be Configured for Designs that do not Require Synthesis





Libero IDE Project Flow Window Synthesis Not Required





Libero IDE Log Window Error Manager

- Error Manager Consists of Tabs in Log Window:
 - All: Displays All Messages
 - Errors: Displays Error Messages
 - Warnings: Displays Warning Messages
 - Info: Displays Information Messages
- Default Error Message Colors can be Changed





Libero error manager tabs Actel Corporation Confidential © 2009

Libero IDE Information Window

Displays New Features in Libero and File Properties





Creating a Libero Project

Libero IDE New Project Wizard

- Menu-Driven Wizard
 - Project > New Project
- Status Guide Shows Current State
 - All Fields Must Be Filled in to Continue
- HDL Type Must Be Consistent with License
- Next Button Goes to Next Wizard Screen
- Finish Button Finishes/Closes Wizard after Making Changes and Saves All Selections

Use Browse button to change project location 、

New Project Wizard		X
Welcom This wizard	e to the New Project Wizard creates a new Libero project.	
Start Select Device	Project <u>n</u> ame:	
Select Tools Add Files	Project location: C:\Actelprj	Browse
	Preferred HDL type: C V <u>e</u> rilog I V <u>H</u> DL	Help
	< Back Next >	Cancel



Libero IDE New Project Wizard Select Device

- Select Family
- After Family Is Selected, Devices from that Family Are Displayed
- After Device Is Selected, Available Packages for Device Are Displayed





Libero IDE New Project Wizard Select Tools

- Synthesis
 - Vendor (e.g. Synplify)
 - Version
- Stimulus
 - WaveFormer Lite
 - Select Version
- Simulation
 - ModelSim
 - Select Version
- Support for Mentor Graphic's Leonardo Spectrum and Precision
 - Standard Tools Direct from Mentor
 - No Actel OEM Versions





Libero IDE New Project Wizard Add Files

- Add Existing Design Files to Project or Create a Link
 - Schematics, Symbols, HDL (VHDL or Verilog), Stimulus (VHDL or Verilog), SmartGen Macros or EDIF Netlists

	Browse to file location
New Project Wizard Add files to you The files are copied Start Select Device Select Tools Add Files Finish Finish	It o your new project files: Files Inks Block Symbol Files (*.[1-9]*) Schematic Files (*.[1-9]*) HDL Source Files (*.vhd; *.v; *.h) Stimulus Files (*.vhd; *.v; *.h) Simulation Files (*.vhd; *.vg) Simulation Files (*.vhd; *.vg) EDIF Netlists (*.edn)
	< Back Next > Finish Cancel



Libero IDE New Project Wizard Finish

- Project Information Listed in Dialog Box
 - Click "Finish" to Complete Project Creation or "Back" to Make Corrections or Additions

New Project Wizard Completi You have st To close thi	ing the New Project Wiza uccessfully completed the New F s wizard and create the project, o	ard Project Wizard. click Finish.	
Start Select Device Select Tools Add Files Finish	The new project will be create Project Name: Project Location: Family, Die, Package: Preferred HDL type: Using Profiles: Stimulus: "WFL" Physical Synthesis: FlashPro: "FlashPr Synthesis: Simulation: 	ed with the following specifications: temp C:\Actelpri\temp ProASIC3, A3P060, 132 QFN VHDL "PALACE" o" "Synplify Pro" "ModelSim SE" Cancel	Project summary shown in window



Organization of Libero IDE Project Files

Actelprj is the Default folder for Libero projects







Libero IDE Project Menu Options





Libero IDE Project Menu Project Settings

8	Project Mana	ger - C:V	Actelprj\L	ibero8.5_te	st\Example	1\Example1.prj *	- [Project Flow]	
8	Project <mark>File E</mark>	dit View	Tools Wi	ndow Help		Project Settings		×
	Project File E New Project. Open Project. Open Project. Save Project. Save Project. Save Project. Detect New I VHDL Library Settings Profiles Configure Pr File Organiza Designer Viel Execute Scrip Preferences. Recent Project Exit	dit View t files oject Elow. ition opt cots	Ctrl+D Ctrl+U	Help		Project Settings Device Flow Simulat Family: ProASIC3 Image: Comparison of the system of th	tion Package: 100 VQFP 132 QFN 144 FBGA 208 POFP 256 FBGA	
							ОК	Cancel Help



Libero IDE Project Settings

- Device Change FPGA die or Package
 - Family cannot be changed

Project Settings		
Device Flow Simulation		
Die: A3P030 A3P060 A3P125 A3P250 M1A3P250 A3P400 A3P600 M1A3P600 M1A3P600 M1A3P1000 M7A3P1000 M1A3P1000	Package: 100 VQFP 132 QFN 144 FBGA 208 PQFP 256 FBGA	
	,	
	ОК	Cancel Help



Libero IDE Project Settings

- Device Change FPGA die or Package
 - Family cannot be changed
- Flow Configure HDL Netlist and DRC Options

Pro	oject Settings 🛛 🔀
D	revice Flow Simulation
	Configure the flow for all modules
	General
	Preferred HDL Type
	⊙ VHDL
	U Verilog
	HDL netlists
	Generate an HDL netlist immediately after Synthesis
	Generate an HDL netlist immediately after Physical Synthesis
	DRC
	Run DRC immediately after Synthesis
	ModelSim
	Update modelsim.ini automatically
	ViewDraw
	 Generate HDL netilist arter a Save&Lneck in ViewDraw Undate viewdraw ini automaticallu
	File detection
	Detect new files on disk automatically
	SmartGen core Generation
	Generate resource report by default
	FlashPro options
	Input programming file for FlashPro:
	O Use STAPL file
	Use PDB file
	Default
_	OK Cancel Help



Libero IDE Project Settings

- Device Change FPGA die or Package
 - Family cannot be changed
- Flow Configure HDL Netlist and DRC Options
- Simulation Specify Simulation Options
 - Simulation run time, testbench name location of do files, etc.

Project Settings		
Device Flow Simulation		
ModelSim options DO File Waveforms Vsim command Hibraries ProASIC3	Name	Value
	Use automatic DO File	
	User defined DO File	
	Simulation runtime	3 ms
	Testbench module name	testbench
	Top level instance name in the testbench	<top>_0</top>
	do command parameters	
	Generate VCD file	V
	VCD file name	power.vcd
		Default
	ОК	Cancel Help



Libero IDE Project Menu Tool Profiles

Specify Tools to Use for Project




OEM Tools Support Tool Profiles

- Create or Edit Tool Profile for Project
 - Project > Profile
 - Select Third-Party Tools & Versions
 - Synthesis
 - Vendor and Version
 - Support for Synplify, Leonardo Spectrum and Precision
 - Simulation
 - ModelSim
 - Select Version
 - Testbench Generation
 - WaveFormer Lite
 - Select Version
 - Name Profile and Save
 - Edit or Add Profiles As Needed





Add / Edit Tool Profiles

- Add/Edit Profile Requires
 - ... Name of Profile
 - ... Choosing Tool
 - From Drop-down Menu
 - Choose Version
 - ... Choosing Tool Location
 - Browse for Location
 - Specify Location

Add Profile			×
Name:			
Select a tool integration:		•	
Version:	LeonardoSpectrum Precision BTI		
Process	Synplify		
Location:			Browse
Additional parameters:			
Restore Defaults	Help	OK	Cancel

Edit Profile	X
Name:	Synplify Pro
Select a tool integration:	Synplify
Version: 8.6.2H	
Process	
Location: D:\Li	bero7.3\Synplify\Synplify_ae_862H\bin\sy Browse
Additional parameters:	
Restore Defaults	Help OK Cancel



Libero IDE Project Settings Files Organization

 Specify Package or Header file Compile Sequence and Stimulus Files and Designer Constraint Files

8	Project Manager - D:\Bootcamp_	1_09\pre-work\Baker\shifter\shifter.prj - [Project Flow]
ନ୍ତ	Project File Edit View Tools Wind	dow Help
[🔥 New Project	≌ ≅ ₩
(🗭 Open Project	
De	<u>C</u> lose Project	× X
5	🛃 Save Project	Design Entry Tools
E	Save Project <u>A</u> s	
	Detect New files Ctrl+D	I/O Attribute HDL Editor SmartDesign ViewDraw
	VHDL Library	
	Se <u>t</u> tings	
	Profiles	Source Files
	Configure Project <u>F</u> low	Jource mes
	File Organization 🔹 🕨	Source Files For Synthesis
	Designer <u>V</u> iews	Source Files For Simulation
L	Exec <u>u</u> te Script Ctrl+U	Synthesis Constraint Files Synplify
	P <u>r</u> eferences	Designer Constraint Files
	Recent Projects	Designer ⊆DB Files…
	E <u>x</u> it	Stimulus
		•



File Organization Source Files for Synthesis

- Project > File Organization > Source Files for Synthesis
- Specify the Order of Synthesis Files in the Project Manager



Manually specify compile order



Uncheck to manually specify synthesis files Actel Corporation Confidential © 2009

File Organization Source Files for Simulation

- Project > File Organization > Source Files for Simulation
- Specify the Order of Project Files for Simulation



Uncheck to manually specify simulation files



Manually specify compile order

Files Organization Designer Constraint Files

- Project > File Organization > Designer Constraint Files
- Specify Designer Constraint Files
 - Timing Constraints (.sdc) or Physical Constraints (.pdc and .gcf)
 - Files may come from Synthesis tool or generated by the engineer





Specify file import

File Organization Stimulus

- Specify Stimulus Files for Simulation
- Libero Supports Hierarchical Testbenches
 - Select Multiple Files
 - Libero Does Not Automatically Determine Compile Dependencies
 of Stimulus Files



Set compile dependencies when testbench contains multiple files



Libero IDE Project Menu Designer Views

- Select Different Views from Menu or Toolbar
 - Check layout results for each Designer view
 - Select from the Current Designer view drop-down menu and run layout

Project Manager - C:\Actelprj\Advanced_VHDL_labs\Solutions\Top\Top.prj	Project Manager - C:\Actelprj\Advanced_VHDL_labs\Solutions\Top\Top.pr
🔗 Project Eile Edit View Tools Window Help	S Project File Edit View Tools Window Help
🖪 🕫 🕅 🗅 🚅 🗆 X 🖻 🕄 😒 😂 🏘 🖨 🎋 🖼 🖓 🖨 🦓 🗖 Enable [🛛 🔁 New Project 2 😂 🏘 🛱 🎲 🖼 🎇 🎒 🦉 🔲 Enable
	C 🐼 Open Project
Current Designer view: Impl2	Des Close Project
Design Explorer Impl Impl2	Save Project Design Entry Tools
Show: Companying Tools	Save Project As
	Detect New files Ctrl+D HDL Editor SmartDesign CoreConsole
	VHDL Library
	Settings
	Profile
	Configure Project Elow
	File Organization
	Designer ⊻iews ► Select ► Im 1
	Everyte Script 🛃 Previous 🗹 In pl2 🔐
	Preferences Interview Inte
	₩ Add
	Cat Remove
	N Exit
	* I * Options1



Libero IDE Designer Views Add, Remove and Edit

Add, Rename or Remove Views

Remove Designer View				
Select the view you want to remove:				
Impl1	•			
1 All the Designer files will be deleted from disk.				
(OK)	Cancel			



Rename Designer View
Select the view you want to rename:
Impl1
Enter the new name:
(OK) Cancel



Libero IDE Project Menu User Preferences

Project File Edit View Tools Window Help	minter smitter.prj - [Project r low]
New Project Close Project Close Project Save Project Save Project As Detect New files Ctrl+D VHDL Library Settings Profiles Configure Project Elow File Organization Designer Views Execute Script Ctrl+U Preferences Recent Projects Exit	Preferences Updates Proxy Startup Log Text Editor Advanced Automatic Software Updates Automatically check for updates at startup Bernind me to check for updates at startup Do not check for updates or remind me at startup Do not check for updates or remind me at startup Do not check for updates or remind me at startup To keep your software up-to-date, you can automatically check for available updates at startup. To manually check for updates. This feature requires an Internet connection. IP Updates Automatic: Automatically download and install cores Standard: Check for updates at startup Manual: Do not remind me at startup



Libero IDE User Preferences Automatic Check for Updates

 Enable or Disable Checking for Software and IP Updates When Libero is Launched





Libero IDE

Checking for Software Updates Manually

Manually Check for Software Updates from Help Menu





Libero IDE User Preferences Text Editor

- Text Editor Selection
 - Use Libero IDE Text Editor or External Text Editor
 - File > Preferences Text Editor Tab

	Preferences 🔀	
Un-check to use external text editor	Updates Proxy Startup Log Text Editor Advanced Use Libero text editor Libero text editor options Replace tab with 4 spaces Open programming/debugging files as read-only User defined text editor	Enter location of
	Location: notepad.exe	— external text editor if selected
	Actel Corporation Confidential © 2009	

48

Libero IDE File Menu Options

💊 Project Manager - C:\Actelprj\Block_Flow_examples\Libero\timing_data_<u>distr\timing_data_distr.p</u> 😣 Project File Edit View Tools Window Help Create, open, 🔥 🗭 🖥 🗋 New... Φ Ctrl+N save and close Current De 😂 Open... Ctrl+O 🔛 🚵 🙋 🖄 🐋 files Close Design Explor Save Ctrl+S а. Show: **Design Entry Tools** Import and Save As.... 1 • • -• **≁**≣ 88 export files Ô М Ē Import Files... 1/0 Attribute SmartDesign HDL Editor ViewDraw ÷....[] Editor Create Link... Change All Links... Unlink All: Copy files locally Source Files Export ٠ Ctrl+P Print... Synthesis Print Preview... G Page Setup... Synplify timing_data_(💌 ė,



Libero IDE File Menu Importing Files

- Existing Design Files Can Be Imported into Libero Project
 - Schematics, Symbols, HDL (VHDL or Verilog), Stimulus (VHDL or Verilog), SmartGen Cores, EDIF Netlists, SDC Files, Constraint Files, Tool Profiles





Project Manager File Linking

- Link External Files to Project
 - Package
 - Source HDL
 - Stimulus
 - Constraint
- Linked File Shows as Blue Text With Icon
- Right Click on Link to Remove or Change





Project Manager File Linking

- Libero Does Not Manage Source File State
 - Linked to file is alterable by project user
 - This may/may not be acceptable by source file owner
- Options:
 - Save the linked source with a new file name
 - Make the Linked to file "read only"
 - Bring (import) the file to the local disk



Project Manager Catalog Options

Download new Cores to IP Catalog



ter:	.		🔎 Search			Select/Uns	ele
	Name	Version	Vendor	Library	Size (MB)	Status	
-	Core429	3.0	Actel	DirectCore	5.2		
~	Core429	3.1.102	Actel	DirectCore	7.3		
-	Core429	3.1.103	Actel	DirectCore	7.3	In Vault	
~	Core429_APB	3.0	Actel	DirectCore	7.1		
-	Core429_APB	3.1.104	Actel	DirectCore	7.1	In Vault	
•	Core1553BRM	3.0	Actel	DirectCore	5.9	In Vault	
-	Core1553BRT	3.1.104	Actel	DirectCore	4.2	In Vault	
-	Core8051s	2.0	Actel	DirectCore	4.5		
	C0051-	0.0.100	A 44-1	Ni	4 5	THE CHARLES	
	Description	www.actel-i Va	ip.com/repositorie ault location is at:	es/DirectCore suc 'D:\Actel\Commo	essfully contaction (Vault'	ed	
ire	Description	www.actei- Vi	ip.com/repositoria ault location is at:	es/DirectCore suc 'D:\Actel\Commo	essfully contacti on\Vault'	ed	
prel	Description	www.actei- Vi	ip.com/repositorie ault location is at:	ss/DirectCore suc	iessfully contacto	ed	



Libero IDE Design Hierarchy

- Libero Displays Design Hierarchy on Hierarchy tab in Design Explorer
- Missing Files Indicated with "?"





Libero IDE File Menu Exporting Files

Export Tool Profiles and TCL Scripts





Libero IDE Edit Menu Options

Copy, Paste, Undo

Find and Replace Add / Remove Comments

Project Mar	ager - D:\Core8051s_	AFS\Libero	o_projects\WHDL\SOC_TOP\SOC_TOP.prj - [Flash4Kx8_wrapper.vhd
Project File	Edit View Tools Windo	w Help	_
🔥 🗭 🛃 [≌ <u>Ω</u> Undo	Ctrl+Z	😥 🥅 Enable Designer Block creation
Current Designer	<u>Ω≅ R</u> edo	Ctrl+Y	
esign Explorer	X Cut	Ctrl+X	
Show: Compo		Ctrl+C	MY_NVM.vhd
🖃 🛒 work	🖪 Paste	Ctrl+V	rary ieee;
	Select Aļļ	Ctrl+A	ity Flash4Kx8_wrapper is
🚊 🔛 SC	Find And Replace	•	port(
	Comment Out Uncomment Out Hash4Kx8_wrapper (I RAM_mux RCOSC100M Shift7	Ctrl+M Ctrl+K 13 14 15 16 17 18 19 20 21 22 23 24 25	CLK : in std_logic; RESET : in std_logic; ADD : in std_logic_vector(1) DATA : in std_logic_vector(3) DOUT : out std_logic_vector(3) DOUT : out std_logic; WIDTH : in std_logic; DISCARD_PAGE : in std_logic; DISCARD_PAGE : in std_logic; ERASE_PAGE : in std_logic; OVERWRITE_PAGE : in std_logic; OVERWRITE_PAGE : in std_logic; PAGELOSS_PROT : in std_logic; READ : in std_logic; READ : in std_logic; READ_NEXT : in std_logic; VIDTA : in std_logic; NUMENTE : in std_logic; NUMENTE : in std_logic; READ : in std_logic; NUMENTE : in s
		Project F	Flow Flash4K×8
		× # -	Text * OPrevious Next A



Libero IDE Edit Menu Find in Files

- Edit => Find and Replace
 - Search for Files, Words, etc
 - Specify by File Types
 - Specify where to Search
 - Text editor, files in project, modules in project
 - Match Whole Word
 - Match Case
 - Regular Expression
- Results Shown in "Search Results" Tab in Log Window

×	entity	🕜 Previous 📀 Next 🔎 Mark All 🏟 🗸 🤇	Options
Window the x	 Find Ports in SmartDesign Find Nets in SmartDesign Find Instances in SmartDesign Find Text in Text Editor Search in Files Search Modules in Project 		Match case Match whole word Overwrite previous results C Append to previous results Existing Pane C New Pane Search Results 1 Close
8	▲ ▲ All 〈 Errors 〉 Warnings 〉 Info 〉	Search Results 1 /	



Find in Files Cross Probing

- Selecting File Name Presented in Find in Files Log Window ...
 - ... Opens Selected File in Libero Text Editor
 - ... Highlights Match





Libero IDE Edit Menu Comment

 Comment Command Allows Users to Comment Sections of VHDL or Verilog HDL





Libero IDE Edit Menu Comment

 Comment Command Allows Users to Comment Sections of VHDL or Verilog HDL





Libero IDE Edit Menu Comment

 Comment Command Allows Users to Comment Sections of VHDL or Verilog HDL





Libero IDE Edit Menu Uncomment

 Uncomment Command Allows Users to Uncomment Sections of VHDL or Verilog HDL





Libero IDE Edit Menu Uncomment

 Uncomment Command Allows Users to Uncomment Sections of VHDL or Verilog HDL





Libero IDE Project Manager View Options

Enable / Disable Windows and Docking Bars

Project Manager - D:\Core8051s_AFS\Libero_projects\	/HDL\SOC_TOP\SOC_TOP.prj - [Flash4Kx8_wrapper.vhd *]	
Project File Edit View Tools Window Help		×
🖪 🐼 🛃 🗋 🚔 Ioolbars	Status Bar	
Image: Project Field Construction Image: Project Field Construction Current Designer view: Project Flow Window Design Explorer Project Flow Window to the front Show: Components Refresh Design Hierarchy Image: Work Reset Window Layout Reset Window Layout Image: Construction Reset Window Layout Reset Window Layout Reset Window Layout Image: Construction Reset Window Layout Reset Window Layo	<pre>> ✓ Status Bar ✓ Standard ✓ Designer Views F2 Ctrl+R ✓ Design Explorer Catalog Information Window trl+W K SET D Configure Information Window Configure Information Window Configure Information Window Catalog Display Options TA Catalog Display Options UT Catalog Display Options Catalog Display Option</pre>	
20 00 21 Pi 22 Pi 23 Ri 24 Ri 25 I (ERWRITE_FROT : in std_logic; GELOSS_PROT : in std_logic; OGRAM : in std_logic; AD : in std_logic; AD_NEXT : in std_logic; CV : in std_logic;	
	ARE_PAGE : in std_logic;	>



Libero View Options Maximize Work Area

POWER

Closes all Other Toolbars to Maximize Working Area

Project File Edt Vew Took Window Help Image: Selection Store Components Bright Heardhy Cubic Store Store Cubic Store Store Components	Project Manager - D:\Actelprj\Q3_08	8_certification\McCarthy\Verilog\SOC_TOP\SOC_TOP.prj - [Flash4Kx8_wrapper.v]	
Image: Solution Topologics Topologics Topologics Image: Explore the Window Bit phote: How Window	Roject File Edit View Tools Window	Help	_ 8 >
Current Deligner wer Page Explore Werg Project How Window to the front P2 Brown Components Werg Project How Window Layout Werg Project How Window Layout	🖪 🐼 🗭 🗋 🖆 <u>I</u> oolbars	► Block creation	
<pre>Project Manager New F Project N</pre>	Image: Solution of the second sec	<pre>> Block creation > Vindow to the front F2 archy Ctrl+R ut Ctrl+W 23, 2008: Written 23, 2008: Written 23, 2008: Written 23, 2008: Written 23, 2008: Written 23, 2008: Written 24, 2008: Written 25, 2008: Written 26, 27, 2008: Written 27, 2008: Written 28, 2008: Written 29, 2008: Written 20, 2008:</pre>	Catalog ↓ ▲ ★ Filter: * Add Core Options △ Function, Name: Version: ● Actel Cells • ● Actel Cells • ● Basic Blocks • ● Else Interfaces • ● Else Interfaces • ● Fusion Perip • ● Feripherals • ● Peripherals • ● C Descriptions Information Window ↓ ▲ ★
Image: Second		Input [31:0] DATA Input [1:0] DATA Project Flow Flash4Kx8	Project Manager New F@ SmartDesign Enhanced Canvas Tesbench generation Datasheet / Memory Map gen Modify Memory Map dialog EDIF Flow Enhanced Find Bar
ide all toolbars to maximize workspace area DEE: AF5600 PKG: 256 FBGA	Hierarchy	D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\Pgm_RAM4 D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\RAM4Kx8\ D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\RAM4Kx8\ D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\RAM_mux\ D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\RAM5C100 D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\Shift7\S D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\Shift7\S D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\Shift7\S D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\smartgen\Shift7\S D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\stimulus\TM_testb 48 occurences have been found.	Properties () File Path: D:\\Flash4Kx8_wrapper.v Library: work Created: Sat Aug 23 22:: Last Modified: Sun Aug 24 02:
	iide all toolbars to maximize workspace area	VERILOG FAM:	Fusion DIE: AF5600 PKG: 256 FBGA

Libero View Options Maximize Work Area (cont.)

Editor Maximized

🐝 🖉 🔂 🔁 🚰 🖌 🛍 🛍 🗠 🖂 🎬 🏗 Enable Designer Block creation	
Current Designer view: Impl1 📃 🛃 🕍 🖄 🖄	
01 02 // Company: Actel Corporation 03 // 04 // File: Elash4Kx8 wrapper v	
05 // File history: 06 // 1.0: August 23, 2008: Written 07 // Description: 08 //	
10 // wrapper to allow Fusion data storage client to be used 10 // in SmartDesign without adding Flash bus interface 11 // 12 // Targeted device: Fusion AFS600 BG265	
13 // Author: Tim McCarthy 14 // 15 /////////////////////////////////	
17 module Flash4Kx8_wrapper (CLK, RESET, ADD, DATA, DOUT, NVM_BUSY, WIDTH, AUX_BLOCK, DISCARD_PAGE, ERASE_PAGE, OVERWRITE_PAGE, OVERWRITE_PROT, FAGELOSS_PROT, PROGRAM, READ, READ_NEXT, LOCK, SPARE_PAGE, UNPROT_PAGE, WRITE, PAGE_STATUS, NVM_STATUS); 19 SPARE_PAGE, UNPROT_PAGE, WRITE, PAGE_STATUS, NVM_STATUS);	
<pre>21 // Inputs 22 input CLK; 23 input RESET; 24 input [17:0] ADD; 25 input [31:0] DATA;</pre>	
<pre>26 input [1:0] WIDTH; 27 input AUX_BLOCK; 28 input DISCARD_PAGE; 29 input ERASE_PAGE; 30 input OVERWRITE PAGE;</pre>	
31 input OVERWRITE_PROT; 32 input PAGELOSS_PROT; 33 input PROGRAM; 34 input READ;	
36 input READ_NEXT; 36 input LOCK; 37 input SPARE_PAGE; 38 input UNPROT_PAGE;	
Project Flow Flash4K×8	
× Mark All Mark All Mark All Mark All	
Ready	AFS600

Libero View Options **Restore Work Area**

Restore Toolbars by Selecting "Restore Work Area"

Project Manager - D:\Actelprj\Q3_08_certification\McCarthy\Verilog\SOC_TOP\SOC_TOP.prj - [Flash4Kx8_wrapper.v]
■ Project File Edit <u>View</u> Tools Window Help
Image: Image
Current Designer view: Project Flow Window
Bring Project Flow Window to the front F2
02 // Compan 03 // 03 //
04 // File: 05 // File h Reset Window Layout
06 // 1 07 // Descrite Work Area Ctrl+W
08 // The storage client to be used
10 // in SmartDesign without adding Flash bus interface
12 // Targeted device: Fusion AFS600 BG265
14 // Author. Tim medarthy
17 module Flash4Kx8_wrapper (CLK, RESET, ADD, DATA, DOUT, NVM_BUSY, WIDTH, AUX_BLOCK, DISCARD_PAGE, ERASE_PAGE, OVERWRITE_PAGE, OVERWRITE_PROT, PAGELOSS_PROT, PROGRAM, READ, READ_NEXT, LOCK, 18 OVERWRITE_PAGE, OVERWRITE_PROT, PAGELOSS_PROT, PROGRAM, READ, READ_NEXT, LOCK,
19 SPARE_PAGĒ, UNPROT_PAGE, WRITE, PAGE_STATUS, NVM_STATUS);
21 // Inputs 22 input CIV:
23 input RESET; 24 input [12:0] ADD:
25 input [31:0] DATA;
27 input [1:0] WIDTH; 27 input AUX_BLOCK;
28 input DISCARD_PAGE; 29 input ERASE_PAGE;
30 input OVERWRITE_PAGE; 31 input OVERWRITE_PROT:
32 input PAGELOSS_FROT; 33 input PROGRAM:
34 input READ; 35. Jonut READ NEWT;
36 input LOCK
38 input UNPROT_PAGE;
Project Flow Flash4Kx8
× ∰ → Text endmodule S Previous S Next Mark All ∰ → Options
estore toolbars

Libero IDE Online Help

HTML-based Help System

- Help Available for Error Messages, Specific Screens and Menus
- Hyperlinks to Application Notes and Actel Web Pages
- Help Menu Provides Direct Access to All Libero PDF Reference Manuals







Libero IDE Design Flows

Libero IDE Design Flows

Structural Schematic Flow

- Contains only Actel ViewDraw Library Components or Mix of Actel ViewDraw Library Components and Structural HDL
- Top Level *Must* Be Schematic!
- Synthesis Optional before Layout
- Mixed-Mode Flow
 - Schematic and RTL Blocks
 - May also Contain Structural HDL Blocks
 - Top Level Must Be Schematic!
 - Synthesis Required before Layout
- HDL Flow
 - Mixed VHDL and Verilog Support in Libero 8.5
 - Requires Synplify Pro AE and ModelSim PE/SE
 - May Contain Structural Blocks



SmartGen Macro Builder
SmartGen Macro Builder

- Create Macro Functions from User's Parameters
 - Multiplexors, counters, memory elements, counters, comparators and I/O macros
 - Supports generation and configuration of Fusion peripherals
- Macros are Optimized for Actel Architecture
 - High Speed
 - Small Area
- Rule-based Generation Guarantees Functional Accuracy
- Outputs:
 - Structural VHDL or Verilog (all macros)
 - Behavioral VHDL and Verilog (most macros)



Using SmartGen Macros

- SmartGen Macros Can Be Used in ...
 - ... Structural Schematic flow
 - ... Mixed-mode Flow
 - ... HDL Flow



Using SmartGen within Libero

- Steps:
 - Launch SmartGen from Libero IDE Project Manager
 - Create HDL Structural Implementation
 - VHDL or Verilog
 - HDL Flow
 - Instantiate Macro in Top-level RTL
 - Structural Schematic and Mixed-mode Flows
 - Create ViewDraw Symbol from Libero
 - Instantiate Symbol in Schematic



Launching SmartGen from Libero

- SmartGen is Integrated into Libero IDE
 - No Separate SmartGen tool in Libero
 - SmartGen Catalog Embedded in Libero Catalog Windows
 - SmartGen Generated Components Managed by Libero Seamlessly





SmartGen Counter Example

Choose Function to Open SmartGen Create Core Dialog box





SmartGen Counter Example

Select type 🔍	Counters : Create Core				
and variation	Linear Pseudo Random Modulo Gray Coun	ter			
	Variations FC Ripple Width Ripple Fast Balanced Register Look Ahead				
	Async Clear Active Low Active High None Clock Rising Falling	Direction © Up © Down © UpDown Count Enable © Active Low © Active High			
	Async Preset Active Low Active High None Generate Reset	Sync Load C Active Low Active High C None Help Close			



SmartGen Counter Example

POWER MATTER



SmartGen Component Generation





SmartGen Family Specific Features: Fusion / ProASIC3 / Axcelerator

- BusLVDS Macro
 - Available for Fusion and ProASIC3
- Visual Configurator for Two-Port and Dual Port RAMs
 - Available for Fusion / ProASIC3 and Axcelerator
- Soft FIFO Controller
 - Available for Fusion / ProASIC3 and Axcelerator
 - Create Controller with or without Memory
- Dynamic Clock Conditioning Circuitry (CCC) Support
 - Dynamically change the CCC configuration by entering the control data serially
 - ProASIC3 and Fusion



SmartGen RAM Visual Configurator



Dual-Port RAM Configurator

Two-Port RAM Configurator



SmartGen ProASIC3 PLL Configurator





SmartGen Fusion Peripheral Support

- SmartGen Includes "System Builders" For Actel Fusion Peripherals
 - Analog Peripherals
 - Flash Memory Blocks
 - FlashROM
 - Easy Customization via Visual Configurators



SmartGen Fusion Analog System Builder

- Fusion "Analog System Builder" category selection and configuration
- Intuitive menu for peripheral selection and configuration

🐁 smartgen.aws - SmartGen									
File Core Options View Help									
🗅 🖨 🛃 🎁 🎗									
Eusion	[]	Core Varieties fi	or Analog System Builder						
📄 🟧 Analog System Builder		Variety		Function	Vendor	Version	Details		
🚽 🗐 Analog System Builder		📕 Analog Sy	stem Builder	Analog System	Actel	1.0	Analog System Builder		
🗄 🖽 Clock Conditioning / PLL									
🗄 📲 Comparators									
🔁 🕂 Counters									
🗎 🕂 🕂 Decoder									
🗄 🙀 FIFO									
🕀 🤣 Flash Memory System Builder	Analog System Build	er							
ElashROM	- ADC Configuration -								
⊞ % I/O	Custom Clarks		Devel March	Les Line					
	System Clock:	MHZ	Resolution:						
			- I						
	Available peripheral	s: Hei	ipnerals used in system	:		-			
Hima Register	Voltage Monitor		A Desistant					bling Rate	Dealers
The second secon	Temperature Monit	or 📕	Peripherai	Sala	ot.			(sps)	Раскад
	Direct Digital Input	· /		Jele	UL				
	Gate Driver								
	Real time Counter			Volta	ane	\mathbf{M}	onitor		
					Jgc				
			•	A	4				
				Curr	eni		onitor		
	Aug to syste	0.0000		Tam			1404		
				lem	D IV	ΙΟΠ	litor		
Categories Alphabetic 🎎 IP Catal					_				
				Diro	rt C		ital Innut		
Name Category Euroctio					J L	лy	παι πηραι		
Rano Catogoly Fanoto						-	-		
				l Gate	Dr	'ĪVe	r		
				Deal			O +		
le l				l Real		ne	Counter		
2						_			
8									
			Modify Sampling Sequer	nce					Genera
б.		_	and a surface of a						
3	Help								Г
Worksnace C: Actelnri Fusion2									L
 server a server a s									

To greate a gora " places double_gligb a gore variaty in the Core Variaty View



SmartGen Fusion Flash Memory System Builder





Structural and Mixed-Mode Flow Using RTL and SmartGen Macros

- Create RTL from Libero HDL Editor or Import File
 OR
- Create HDL Structural Implementation using SmartGen
 - VHDL or Verilog
- Create ViewDraw Symbol from Libero and Instantiate Symbol in Schematic
 - Symbol Appears on Files Tab



Structural Schematic Designs

Structural Schematic Design Flow





ViewDraw Overview

Opening ViewDraw

- Click ViewDraw Button in Project Flow Window
- Create Schematic
- Save and Check

Design Entry Tools			
■	■	♥	
HDL Editor	MartDesign	ViewDraw	





ViewDraw GUI





Adding Schematic Components

- Add > Component from ViewDraw Menu
 - Add SmartGen Macros, Custom Macros or Actel Basic Cells
 - Select VCC or GND from 'actelcells'





Adding I/O Cells

- Add I/O Cells to Top-level Design Schematic
 - Schematic-only Designs or Structural Schematic Designs
 - Macros Contained in "actelcells" Component Library
- I/O Cells Must Have Dangling Hierarchical Connector Attached to Pad Side
 - Label Dangling Connector
- I/O Macros Can Be Buried in Hierarchy





Drawing Wires and Busses Adding a Net

- To Add Net:
 - Choose Add > Net (or Add > Bus)
 - Alternate: Click Wire (→) or Bus (→) Icon on Toolbar
 - Specify Net Origination Point and Depress Left Mouse Button
 - Drag Mouse to Form Net (or Bus), specifying Points along Net by Clicking Right Mouse Button
 - Click Right Mouse Button to Insert Vertex in Net
 - Release Left Mouse Button to Specify Ending Point for Net



Hierarchical Connectors

- Use Hierarchical Connectors from ViewDraw Built-in Library for All Designs
 - Add just like Any Other Component
 - Same Connector for Wire or Bus
 - Called 'in', 'out', or 'bi' in Built-in Library
- Label Net or Bus Next to Connector







ViewDraw Attributes

- A Limited Number of Attributes Can Be Entered into Schematic and Passed to Designer
- \$Array Attribute
 - Creates Arrays of Cells in Schematic
 - Useful for I/O Buffers
 - Double-click Cell, Enter on Attribute Tab







Completed Schematic





Design Rule Checking

- At Design Entry Completion , Save and Check Design
 - Click Save Check Icon
 - Use Tools > Schematic Checker

Basic Results Current Project: Schematic Name mux2_1 Process to Run © Check the design specified and all of the hierarchy. (Default) © Check only the sheet specified. © Check all writable schematics in all writable directories. Processing Option © Display more status messages as checking occurs. (Verbose)	🗸 Schematic Checker 🛛 🔀					
Current Project: Schematic Name mux2_1 Process to Run Check the design specified and all of the hierarchy. (Default) Check only the sheet specified. Check only the sheet specified. Check all writable schematics in all writable directories. Processing Option Display more status messages as checking occurs. (Verbose)	Basic Results					
Schematic Name mux2_1 Process to Run Check the design specified and all of the hierarchy. (Default) Check only the sheet specified. Check all writable schematics in all writable directories. Processing Option Display more status messages as checking occurs. (Verbose) 	Current Project:					
mux2_1 Process to Run Check the design specified and all of the hierarchy. (Default) Check only the sheet specified. Check all writable schematics in all writable directories. Processing Option Display more status messages as checking occurs. (Verbose) 	Schematic Name					
Process to Run Check the design specified and all of the hierarchy. (Default) Check only the sheet specified. Check all writable schematics in all writable directories. Processing Option Display more status messages as checking occurs. (Verbose)						
 Check the design specified and all of the hierarchy. (Default) Check only the sheet specified. Check all writable schematics in all writable directories. Processing Option Display more status messages as checking occurs. (Verbose)	Process to Run					
 Check only the sheet specified. Check all writable schematics in all writable directories. Processing Option Display more status messages as checking occurs. (Verbose) 	$(\ensuremath{\widehat{\bullet}}\xspace$ Check the design specified and all of the hierarchy. (Default)					
 Check all writable schematics in all writable directories. Processing Option Display more status messages as checking occurs. (Verbose) 	C Check only the sheet specified.					
Processing Option	C Check all writable schematics in all writable directories.					
	Processing Option					
	Run Close Help					

🗸 Schematic Checker	
Basic Results	
CHECK examines each schematic for m	inor connectivity violations.
(Any output errors must be resolved ber	📱 ViewDRC
additional connectivity and design rule	Design Settings Severities Results
	Using ini file D:\Actel\Libero_v8.5\viewdraw\standard\vdrc.ini Loading Design mux2_1 Loading Design mux2_1 done, 0.02 seconds Running design rule checks. Running design rule checks done, 0 seconds 1 message disabled, viewable with 'Show Disabled'. 1 error, 2 warnings, 0 notes written to C:\Actelpri\ViewDraw_example\viewdraw\mux2_1.drc NoPinCon: Warning: MUX2_1 com \$113: No connected output pins NoInPinCon: Error: MUX2_1 com \$116: No connected input pins InPinCon: Warning: MUX2_1 pin \$116.D: Unconnected input pins
	DRC Check Results
	Clear Summary Run Cancel Defaults Help
Chan Commun. History Toron	Decion Pula Chacker
	Run Close Help



Design Entry Completion

 Files in Implementation are Displayed on Libero Hierarchy and Files Tabs





ViewDraw File Structure on HDD

- Schematic Files Saved in "sch" Folder
- Symbol Files Saved in "sym" Folder
- Wire Files Saved in "wir" Folder
- Files Visible on Libero File Manager Tab







Libero Schematic Checker (Optional)

- Schematic Connectivity Checker in Libero
 - Checks for Errors Not Included in ViewDraw Save + Check
 - Optional Step Available from File Manager Tab





Opening Existing Schematics

POWER



Mixed-Mode Designs

Mixed-Mode Design Flow





Mixed Mode Design Entry

- Mixed Mode => RTL Blocks within Schematic
 - HDL Blocks Can Be Structural or Behavioral RTL
 - Libero IDE Supports Mixed VHDL and Verilog Source Files
 - Top Level *Must* Be Schematic
- Procedure
 - Create HDL Blocks
 - RTL Blocks Use HDL Editor or Import Existing Design Files
 - Structural Blocks Use HDL Editor or SmartGen
 - Create ViewDraw Symbols for HDL Blocks
 - Done Automatically from Libero
 - Instantiate Blocks in Schematics and Make Interconnects
 - Use Hierarchical Connectors from ViewDraw "built-in" Library for HDL Ports in Schematic





Structural and Mixed-Mode Flow Using RTL and SmartGen Macros

- Create RTL from Libero HDL Editor or Import File
 OR
- Create HDL Structural Implementation using SmartGen
 - VHDL or Verilog
- Create ViewDraw Symbol from Libero and Instantiate Symbol in Schematic
 - Symbol Appears on Files Tab





Mixed Mode Schematic




Synthesis

- Optional for Pure Schematic or Structural Schematic Flows
 - All HDL Blocks Are Structural VHDL or Verilog (e.g., SmartGen Blocks)
- Required for Mixed-mode Designs
 - Designs Containing RTL Blocks
- Libero Launches Synplicity to Insert Pads and Optimize Design
 - Hierarchical Connectors Must Be Used
 - Structural Schematics with All Pads Instantiated Can Go Directly to Designer Tool



HDL Designs

HDL Design Flow





Creating New HDL Macros





HDL Editor

POWER



Inserting HDL Templates

- To Insert Template:
 - Place Insert Cursor Where you want it in the HDL Text Editor
 - Double Click Selected Template or ..
 - Right Click and Select "Copy template to a file"





HDL Templates in Text Editor

Template is Inserted into Text Editor Window





Libero HDL Syntax Checker

HDL Syntax Checker Available from Hierarchy or Files Tab

- Checks for Syntax Errors in HDL Blocks
- Errors Indicated in Libero Log Window
- Optional Step





Deleting Files from Libero Project

- Files Can Be Deleted from Project and from HDD
 - Files Deleted from HDD Cannot Be Recovered!



SmartDesign

What is SmartDesign?

- Powerful Block-based Visual Design Creation Tool
 - Instantiate blocks from a variety of sources
 - DirectCore IP, SmartGen, User HDL, Companion Cores, Actel library cells, and the list goes on.
 - Supported for all platforms
- Simple and Intuitive Design Creation
 - Auto Connect
 - Fast manual connectivity between blocks
 - Hierarchical design support
- DRC
 - Checks rules to guarantee correct by construction design
 - Connectivity errors
 - Configuration errors
 - Special silicon rules
- SOC Features
 - Auto Connect
 - clocks and resets for processors and peripherals
 - Other known DirectCore connections
 - Memory Map Configuration Dialog
 - Testbench and Bus Functional Model (BFM) script generation



Opening SmartDesign

- Click SmartDesign Button in Project Flow Window
- Add and Stitch Blocks
- Generate HDL







SmartDesign Canvas





SmartDesign Canvas Enhancements

SmartDesign Canvas

- Instance pins are displayed on canvas.
- Connections are shown using nets
 - Displaying of Nets is optional
 - Selective enabling / disabling of showing nets
- Drag and Drop directly from the Catalog into the Canvas
- All Design Operations Available in the Canvas
 - Connect / Disconnect
 - Promote To Top
 - Tie Low / Tie High / Tie Constant / Inversion
 - Float
 - Split (if bus)
 - Group



Design with any block types

One Tool to Connect Your Design

- DirectCore IP
- SmartGen Cores
- User HDL
- Actel Macros (And, Or, I/Os, etc)





Canvas Instance





Cores Catalog

- Library of Proven Configurable Core Functions
- Actel Macros
- Quick-find
- Intuitive Configuration
- Drag and drop to Canvas





Actel Corporation Confidential © 2009

Making Connections

- Right-click on a pin for Available Operations
- Select 2 or More Pins With the CTRL key, Right-click and Connect





Modifying Memory Map

- Easy and Intuitive Method to Connect Peripherals at Particular Addresses on the Bus
- Interactive and Immediate Updating of Base Addresses

Modify Memory Map		
Select Bus to View or Assign Peripheral(s)	Assign peripherals to	o addresses on bus:
⊡- CoreAHBLite_0	Address	Peripheral
CoreAPB_0	0x10000000	CoreTimer_0:APBslave
	0x11000000	
	0x12000000	
	0x13000000	
	0x14000000	
	0x15000000	
	0x16000000	
	0x17000000	
	0x18000000	
	0x19000000	CoreUARTapb_0:APBslave
	0x1a000000	
	0x1b000000	
	0x1c000000	
	0x1d000000	
	0x1e000000	
	0x1f000000	
Help	,	OK Cancel



Fast Design Search

- Design Level Search
 - Find Pins, Instances, and Nets quickly and easily
 - Wild card query
 - Matching objects will be highlighted in the Canvas





Multiple Representations of the Design

- Connectivity Grid
 - Spreadsheet like view of your design
 - Enables quick filtering / sorting
- Schematic
 - Shows all pins and nets
 - Traditional schematic view





Design Rule Checker

- Checks your Design for Errors
 - Invoke with Checker icon (see picture)
 - Connectivity
 - Unconnected/Required input pins
 - Floating output pins
 - Silicon required connection
 - Example: RTC must be driven by Crystal Oscillator
 - Configuration
 - Check consistency between configurations
 - Example: CoreMP7 and CoreMP7Bridge debug configuration
- Errors Reported in a Connectivity Grid
 - Directly fix your connectivity mistakes
 - Enables fast sorting / filtering

*	Message	V •	Instance	V	Port Name	V	Slice 🔽	Attribute	SD1
🗄 Floati	ing Driver 🥂								0
Unco	nnected Bus Inter	face 🥂							0
🛛 Undri	iven Pin 🌆 ———		CoreAHBLite	_0	I> Remap				
	-	F	CoreUARTa	ob	IV BX				
		L.	CortexM1T op	0_0				Polnvert	0
								¥ Tie Low	
								Tie High	





Testbench Generation

- Design Testbench
 - Generates a top level testbench
 - Clock and Reset drivers automatically generated and connected
- Bus Functional Model Script Generation
 - Generates BFM script file for processor based designs
 - Based on your peripheral connectivity in your designs
 - Look at Processor Core Handbooks (ex: CortexM1) for more details on BFMs and usage



Datasheet Generation

- Design Datasheet
 - Pin outs of the design
 - Cores used and their description
 - Memory Map

AM: Fusion S ie: M1AFSt S	: <u>oreTimer_0</u> :oreUARTapb_0												
ackage: 484 FBC C	CortexM1Top_0	CoreTimer_0	: RegisterMap	Memory	у Мар								
tate: SAVED	p of page	<i>range:</i> 0×010000	00										
	Instance Name		Address		Туре	Width	Reset Value	Name	Descriptior				
5	Type: Vendor: Library: Core Name: Version: Description: instance list, top of pa		base address + 0x00		read-write	32	0x0000000) <u>TimerLoad</u>					
res mory Map			base address + 0x04		read-only	32	0xFFFFFFFF	TimerValue					
mory map			base address + 0x08		read-write	32	0x00) <u>TimerControl</u>					
			base address + 0x0C		write-only	32	0x0) <u>TimerPrescale</u>					
			base address + 0x10		write-only	32	0x0) <u>TimerIntClr</u>					
			base address + 0x14		read-only	32	0x0) <u>TimerRIS</u>					
in			base address + 0x18		read-only	32	0x0) <u>TimerMIS</u>					
	Instance Name Type:	TimerLoad ı	egister details:										
	Vendor:		Bit Offset	Туре	Bit V	Vidth	Name	Descri	ption				
			0	read-w	rite	32	LoadValue	Load value for co	unter				
	Library:		~	1000011		back to CoreTimer_0 Registers							
	Library: Core Name: Version: Description:	TimerValue	register details:		back	<u>∢ to CoreTim</u>	ner <u>0 Registers</u>						
in	Library: Core Name: Version: Description: stance list, top of pa	TimerValue	register details:	Tripo	back	< to CoreTim	er_O Registers	Deseri	ation				
in	Library: Core Name: Version: Description: stance list, top of pa	TimerValue	register details: Bit Offset	Туре	back Bit Wid	k to CoreTim	Name	Descrij	otion				



SmartGuide Design Guidance

- Identify Silicon Design Rules and Compatibilities
 - Eliminate errors typically detected only at place & route time
 - Example: Using RTC in Fusion requires the Crystal Oscillator
- Detect and Flag Logic Design Errors
 - Eliminate errors typically detected only at synthesis time
 - Un-driven inputs
 - Floating outputs
- Restrict Illegal Choices When Making Connections
 - Direction incompatibilities
 - Dimension mismatches
- Auto-connect Standard Interfaces



SmartGuide Design Management

- Streamline Iterative Design Changes
 - Unique to SmartDesign
 - Detect and flag out-of-date components
 - Assist in component interface updates
 - E.g. Removing connections to a deleted port
- Synchronize Data Between Building Blocks
 - E.g., Flash Memory must be updated because Analog System changed
- Flag the Next Steps For a Design Change
 - Example, Reprogram the Flash Memory region for Boot-Code if a new Boot-Code file is generated
 - Example, Re-synthesize the design if a new Analog peripheral is added to the design



Hands-on Labs 1 and 2

- Complete Labs 1 and 2 in the Lab Guide
- Lab 1
 - Extract Lab Files
 - Create New Libero Project and Import Source Files
- Lab 2
 - Configure FlashROM with SmartGen Save Your Work



Functional Simulation





Simulation Flow

For Each Block You Want to Simulate . . .





Invoking WaveFormer Lite





WaveFormer Lite Features

- Allows Convenient Test Stimulus Specification via GUI
 - User Specifies Stimulus by Drawing Waveforms
 - Supports Copy / Paste / Append Operations
 - Significantly Reduces Testbench Creation Time
 - Automatically Converts Graphical Stimulus Files into HDL TestBenches
 - Can Generate:
 - VHDL Testbench (*.vhd)
 - Verilog Testbench (*.v)
- Users Can Annotate Waveform For Design Documentation



Drawing Stimulus

WaveFormer Lite Diagram Window





.

Right Z			
Click!	\leq		
	CDiagram - untit	led1.btim*	<u> </u>
Y	Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Q + Q F Hold Text Marker Image: Amount of the set of the s	
	14.00ns <mark>14.00ns</mark>	0ns 50ns 100ns 150ns 200ns 250ns 300ns	350ns
	CLK		
	RESETN		
	LOAD		
	ENABLE		
	DATA[15:0]		
	COUNT[15:0]		
	•		◄







M	7		
Double Click!	\leq		
TINN	🔓 Diagram - untit	led1.btim*	_ 🗆 🗙
r V V	Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Hold Text Marker — — — — — — — — — — — — — — — — — — —	
	14.00ns <mark>14.00ns</mark>	0ns 50ns 100ns 150ns 200ns 250ns 300ns	350ns
	CLK		
	RESETn		
	LOAD		
	ENABLE		
	DATA[15:0]		
	COUNT[15:0]		



	Signal Properties	
	Name: CLK	
	Simulate Once Analog Props Grid Lines	
	Tive O Simulate O Watch O Compare	
	elean Equation: ex. (SIG1 and SIG2) delay 5	
dd Signal Ad	lock; Unclocked 🔽 Edge/Level; neg 🔽	
14.00ns 1	Clock Properties Clock Properties Clock Properties Clock Properties Clock Properties	50ns 200ns 250ns 300ns 350r
RE	Boolean Equation C Verilog C VHDL	
L		
EN/	Wim Eqn 8ns=2 (5=1 5=0)*5 9=H 9=L 5=V 💌	
	Label Eqn Hex(Inc(0,2,5))	
	Export Signal Direction: output	
	T Analog Display Size 1	
•	VHDL; std_logic 🔽 Verilog; reg 🔽	
	Radix; hex Bus MSB; 0 LSB; 0	
	🗖 Falling Edge Sensitive 🔲 Rising Edge Sensitive	
	OK Cancel Apply Prev Next	


			Edit Clock Parameters	? ×	1
	Name: CLK		Name CLK		Clock name
	Simulate Once Analog Props Grid Lines		Reference Clk: None	•	
	O Drive O Simulate O Watch O Compare		Freq:	10. • KH2 / us	- Clock
	Boolean Equation: ex. (SIG1 and SIG2) delay 5		Period:	100, O GHz / ps	requency
Add Signal Ad	Clock: Unclocked 💌 Edge/Level; neg 💌		Period Formula: ex. 2*CLK 100	(O.period	
Add Clock Ad 14.00ns 14	Clock Properties	50ns	Starting Offset:	0. 0	1350ns
	Clock Enable: Not Used 🔽 Advanced Register		Duty Cycle %:	50. 50	CIOCK
RE	Boolean Equation O Verilog O VHDL		Rise Jitter (range):	0 0	duty
L	·		Fall Jitter (range):	0 0	cycle
EN/	Wfm Eqn 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V 💌		Buffer Delay		
DATAI	Label Eqn Hex(Inc(0,2,5))		Min L to H:	0 0	
			Max L to H:	0 0	
	Export Signal Direction: output		Min H to L:	0 0	
	T Analog Display Size 1		Max H to L :		-
•	VHDL; std_logic 💌 Verilog; reg 💌		Rising Delay Correlation:	100 %	
	Radix: hex 🔻 Bus MSB; 0 LSB; 0		Falling Delay	100 %	
			Rise to Fall Correlation	100 %	
				//	Start high
	OK Cancel Apply Prev Next		🗖 Invert (Starts Low) 🗲		
		1	ОК	Cancel	



	Signal Droperties	1	Edit Clock Parameters	? ×	
			Name CLK		
	Name: CLK		Reference City None		
	Simulate Once Analog Props Grid Lines				
	C Simulate Watch C Compare		Freq: 50.	◯ KHz / us	
	Boolean Equation: ex. (SIG1 and SIG2) delay 5		Period: 20.	OGHz / ps	
P Diagram	_		Period Formula: ex. 2*CLKO.pe	riod	
Add Signal Ad	Clock; Unclocked 🔽 Edge/Level; neg 🔽		20		
Add Clock Ad	Clock Properties	5000	Starting Offset:	0. 0	1250.00
14.00HS			Duty Cycle %:	50. 50	
			Rise Jitter (range):	0 0	
			Fall Jitter (range):	0 0	I
	Wfm Eqn 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V 🔽		Buffer Delay		<u> </u>
	Label Eqn Hex(Inc(0,2,5))		Min L to H:	0 0	
			Max L to H:	0 0	
	Export Signal Direction: output		Min H to L:	0 0	
	Analog Display		Max H to L:	0 0	-
•	VHDL: std_logic Verilog:	2	Rising Delay Correlation:	100 %	
	Radix: hex Bus MSB Click!	<	Falling Delay	100 %	
			Rise to Fall Correlation:	100 %	
		N			
			Invert (Starts Low)		
			ОК	Cancel	



	Signal Properties	? ×
	Name: CLK	Active Low
	Simulate Once Analog Props G	Grid Lines
	C Drive C Simulate C Watch C	C Compare
	Boolean Equation: ex. (SIG1 and SIG2) dela	alay 5
Add Signal Add	Clock; Unclocked 🔽 Edge/Level;	
Add Clock Add 14.00ns 14.	Clock Properties	50ns 200ns 250ns 300ns 350ns
	Clock Enable; Not Used 🔽 🛛 Advance	
RE	© Boolean Equation 🛛 🔿 Verilog 🔷 🔿	
	Wfm Eqn 8ns=Z (5=1 5=0)*5 9=H 9	9=L 5=V 💌
DATA[Label Eqn Hex(Inc(0,2,5))	•
	Export Signal Direction: output	
VV4	🗖 Analog Display	Size 1
	VHDL; std_logic 🔽 Verilog; reg	
TINT	Radix; hex 🔽 Bus MSB; 0	LSB: 0
	🗖 Falling Edge Sensitive 🛛 🔲 Rising Edg	lge Sensitive
	OK Cancel Apply Prev	Next



🕂 Diagram - untit	tled1.btim*	
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Q + Q F Hold Text Marker Image: Amage: Amage	
14.00ns <mark>14.00ns</mark>	0ns 150ns 1100ns 150ns 1200ns 1250ns 1300ns 1350)ns
CLK	\frown	
RESETn		
LOAD		
ENABLE		
DATA[15:0]		
COUNT[15:0]		
		₋∠
▲		



Select "low" state button

🕂 Diagram - untit	led1.btim* 🖌
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Hold Text Marker — — — — — — — — — — — — — — — — — — —
110.0ns <mark>65.00ns</mark>	0ns <mark>1</mark> 50ns 110 <mark>0ns 1150ns 1200ns 1250ns 1300ns 1350ns</mark>
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	
COUNT[15:0]	
◀ ▶	 ▲



Toggle state $-\Box \times$ 🕂 Diagram - untitled1.btim* **Q + Q**F **Q - Q**R Add Signal Add Bus Delay Setup Sample ніĠн VAL INVAL WHI WLO HEX Hold Text Marker Add Clock Add Spacer [200ns |250ns 110.0ns 65.00ns 0ns (50ns 10<mark>0ns</mark> |150ns |300ns |350ns CLK RESETn LOAD ENABLE DATA[15:0] COUNT[15:0] ▶ | ◄ •



State button toggles automatically

🕂 Diagram - unti	tled1.btim*		_ 🗆 🗵
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample Hold Text Marker		
118.0ns <mark>54.00ns</mark>	10ns 150ns	100rs 150ns 200ns 250ns 300ns	350ns
CLK			
RESETn			
LOAD	†		
ENABLE			
DATA[15:0]			
COUNT[15:0]			
	•		▼ ▶



Align courser and click! Use zoom controls to make viewing easier



🕂 Diagram - until	tled1.btim [*]	
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO Hold Text Marker - TRI VAL INVal WHI WLO HEX Q - Q R	
118.0ns <mark>54.00ns</mark>	0ns 50ns 100n <mark>s 150ns 200ns 250ns 300ns 35</mark>	ions
CLK	$\wedge \wedge $	∕∖_
RESETn		_
LOAD		<u>† </u>
ENABLE		
DATA[15:0]		
COUNT[15:0]		
•	<u>۱</u>	▼ ▶ //

Align courser and click! Use zoom controls to make viewing easier



Drawing Signals Edge Placement

🕂 Diagram - untit	led1.btim*			
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH			
118.0ns 54.00ns	Edge Properties	····	200ns 250ns 300ns	350ns
CLK RESETn LOAD ENABLE DATA[15:0] COUNT[15:0]	Edge Placement Min: 365 Max: 365 Min Uncertainty: 0 Uncertainty =0 ns Locked OK Cancel	Multiple Delay Resolution ● Default ● Earliest Transitions ● Latest Transitions ● Max Uncertainty ● Min Uncertainty ● Driven (for inout signals only) Apply Prev		
	•			• •
Enter tim	e for edge placen	nent	Double click at end of signal	



💁 WaveFormer Lite -	WaveFormer Lite - [Diagram - untitled1.btim*]				
귺 Eile Export Edit (Bus ParameterLibs Report View Options Window Help				
🛛 🖻 🖬 🖨 🎒	• • •				
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO Hold Text Marker - TRI VAL INVal WHI WLO				
202.0ns 35.00ns	Ons 50ns 100ns 150ns 200ns 250ns 300ns 350ns				
CLK					
RESETn					
LOAD					
ENABLE					
DATA[15:0]					
COUNT[15:0]					
Click to draw wavef	orm displayed on red state button Simulation Inactive				



💁 WaveFormer Lite -	[Diagram - untitled1.btim*]
귺 Eile Export Edit (Bus ParameterLibs Report View Options Window Help
🛛 🖻 🖬 🎒 🎒	
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO Hold Text Marker - TRI VAL INVal WHI WLO HEX Q - Q R
210.0ns 18.00ns	Ons 50ns 100ns 150ns 200ns 250ns 300ns 300ns 350ns
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	
COUNT[15:0]	
	Simulation Inactive



💁 WaveFormer Lite -	[Diagram - untitled1.btim*]
귺 Eile Export Edit §	Bus ParameterLibs Report View Options Window Help
🛛 😅 🖬 🕼 🎒 🎒	<u>_</u>
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Q+ QF Hold Text Marker
152.0ns <mark>-40.00ns</mark>	Ons 50ns 100ns 150ns 200ns 250ns 300ns 350ns
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	
COUNT[15:0]	
	Simulation Inactive



🤷 WaveFormer 🛛	Lite - [Diagram - untitled1.btim*]			l ×
🕂 File Export	Edit Bus ParameterLibs Report View	v Options	ns Window Help	$1 \times$
] 🛩 🖬 🎒 (Undo Change Segment State Redo ClearRedEvents	Ctrl+Z Ctrl+Y		
Add Signal Add	Delete	Del	VAL INVALWHI WLO HEX 9+9F	
Add Clock Add	Clear Red Events			
63.00ns -12	Copy Ole Image To Clipboard \w save Copy Ole View To Clipboard \w save Copy To Clipboard		s, , , , , , , , , , , , , , , , , , ,	
RE	Cut Signals/Text Select All Signals	Ctrl+X Ctrl+A		
EN.	Copy Signals Paste Signals	Ctrl+C Ctrl+V		
DATA	Block Copy Waveforms			
COUNT	Edit Clock Insert Clock Cycles Delete Clock Cycles Right Click Delete Mode			-
Clear same s	Edit Text, (Un)Lock Edges of Selected Signals	+	Simulation Inactive	



💁 WaveFormer Lite -	[Diagram - untitled1.btim*]
귺 Eile Export Edit (Bus ParameterLibs Report View Options Window Help
🛛 😅 🖬 🕼 🎒	QQ
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO Hold Text Marker - HIGH LOW TRI VAL INVal WHI WLO
129.0ns <mark>-63.00ns</mark>	Ons 50ns 100ns 150ns 200ns 250ns 300ns 350ns
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	
COUNT[15:0]	
	Simulation Inactive



🕂 Diagram - untitled	1.btim*
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI WLO HEX Q+ QF Hold Text Marker - C - C - C - C - C - C - C - C - C -
163.0ns 4.000ns	0ns150ns1100ns115 <mark>0</mark> ns1200ns1250ns1300ns1350ns
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	
COUNT[15:0]	

Double click "VAL" state button



<mark>G</mark> Diagram - untitled	1.btim*
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI HEX Q + Q F Hold Text Marker Image: Setup Im
163.0ns 4.000ns	0ns 150ns 100ns 13 <mark>0</mark> ns 1200ns 1250ns 1300ns 1350ns
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	
COUNT[15:0]	

Button will stay in "VAL" state



🔓 Diagram - untitled	I.btim*
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI WLO HEX Q + Q F Hold Text Marker Image: Comparison of the set of t
163.0ns 4.000ns	0ns150ns1100ns1150ns1200ns1250ns1300ns1350ns
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	
COUNT[15:0]	



🕂 Diagram - untitled	I.btim*
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI WLO HEX Q + Q F Hold Text Marker INVal WHI WLO HEX Q - Q R
163.0ns 4.000ns	0ns150ns1100ns1150ns1200ns1250ns1300ns1350ns
CLK	
RESETn	
LOAD	
ENABLE	
DATA[15:0]	χ
COUNT[15:0]	1



🕂 Diagram - untitled)	l.btim*
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVAI WHI WLO HEX Q + Q F Hold Text Marker - C Simple Simple Setup Constraints of the setup Setu
163.0ns 4.000ns	0ns150ns1100ns1150ns1200ns1250ns1300ns1350ns
CLK	
RESETN	
LOAD	
ENABLE	
DATA[15:0]	<u> </u>
COUNT[15:0]	





🕂 Diagram - untitled	l.btim*	
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI WLO HEX Q+ Q Hold Text Marker	
163.0ns 4.000ns	0ns150ns1100ns1150ns1200ns	250ns 300ns 350ns
CLK		
RESETn		
LOAD		Virtual:
ENABLE		Hadix: hex(default)
DATA[15:0]	χ	
COUNT[15:0]		Binary; V
		<= Prev OK Next =>
I		



🕂 Diagram - untitled 1	l.btim*	
Add Signal Add Bus Add Clock Add Spacer	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	
163.0ns 4.000ns	10ns 150ns 7 1100ns 150ns 1200ns 1	250ns 1300ns 1350ns
CLK		
RESETn		
LOAD		Virtual: AAAA
ENABLE		Hadix: hex(default)
DATA[15:0])	Pierre V
COUNT[15:0]		Driven (for inout signals only)
		<= Prev OK Next =>





🕂 Diagram - untitled	I.btim*	
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI WLO HEX Q+ Q Hold Text Marker	
163.0ns 4.000ns	10ns 150ns 1100ns 150ns 1200ns 12	250ns 300ns 350ns
CLK		
RESETN		
LOAD		Virtual:
ENABLE		Hadix: hex(default)
DATA[15:0]		Pipour V
COUNT[15:0]		Driven (for inout signals only)
		<= <u>P</u> rev OK <u>N</u> ext ⇒



🕂 Diagram - untitled	1.btim*	
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI WLO HEX Q + Q F Hold Text Marker Image: Constraint of the set of t	
163.0ns 4.000ns	10ns 150ns 1100ns 150ns 1200ns 12	250ns 1300ns 1350ns
CLK		
RESETN		
LOAD		Virtual: BBBB
ENABLE		Radix: hex(default)
DATA[15:0]		
COUNT[15:0]		Diriary: Jv
	•	<= Prev OK Next =>





🕂 Diagram - untitled)	l.btim*
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LOW TRI VÁL INVal WHI WLO HEX Q + Q F Hold Text Marker - Q - Q R
163.0ns 4.000ns	0ns150ns1100ns1150ns1200ns1250ns1300ns1350ns
CLK	
RESETN	
LOAD	
ENABLE	
DATA[15:0]	AAAA (BBBB
COUNT[15:0]	



💁 WaveFormer Lite
File Export Edit Bus ParameterLibs Report View Options Window Help
≥
☐ Diagram - untitled1.btim*
Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VÅL INVal WHI WLO HEX Q + Q F Add Clock Add Spacer Hold Text Marker -// -// -// -// -// N/al WHI WLO HEX Q - Q R
2.000ns 179.0ns Dns 50ns 100ns 150ns 200ns 250ns 300ns 350ns
RESETN
LOAD
ENABLE
DATA[15:0] AAAA X BBBB
COUNT[15:0]
Add a new bus or merge the selected signals into a bus Simulation Inactive



💁 WaveFormer Lite
File Export Edit Bus ParameterLibs Report View Options Window Help
☞ 日 日 鼎 雪 」 ④ ④ ④ ④
C Diagram - untitled1.btim*
Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VÅL INVal WHI WLO HEX Q + Q + Add Clock Add Spacer Hold Text Marker WHI WLO HEX
1.000ns 180.0ns 0ns 50ns 100ns 150ns 200ns 250ns 300ns 350ns
RESETN
LOAD
ENABLE
DATA[15:0] AAAA (BBBB
COUNT[15:0]
Simulation Inactive



ø:w	aveForn	her Lite								
File	Export	Edit Bus	ParameterLibs	Report	View	Options	Window	Help		
🚅		Undo Ed	lit Bus		Ct	rl+Z				
		Redo			Ct	rl+Y				
l 🔐	Diagram	Delete			De	9				
Add 9 Add 0	Signal Ad Clock Ad	Clear Re	d Events]	YHI WLO	HEX	<u>२</u> + ० २- ०	QF QR
40.0	0ns 14	Copy Ok	e Image To Clipbo	oard ∖w sa	ve	ſ	1150ns 🗸	120)0ns	250ns 300ns 350ns
		Сору Ок	e view To Clipboa Voliaia and	ira (wisavi	e	-				
⊫		Сору то) Cippoard				$\overline{\cup \cup}$	\Box		
	RE	Cut Sign	als/Text		Ct	rl+X				_
	L	Select All	l Signals		Ct	rl+A				
	ENL	Copy Sig	gnals		Ct	rl+C				
		Paste Sig	gnals		Ct	rl+V				
	DATA[Block Co	py Waveforms				<u>X</u> E	BBB		
	COUNT	Edit Cloc	:k							
		Insert Cl	ock Cycles							
		Delete C	lock Cycles							-
•		Right Clie	ck Delete Mode							
Co	pies the	Edit Text	t k Edges of Select	ed Signals		•	signals			Simulation Inactive



	Block Copy Waveforms	? X	
WaveFormer Lite File Export Edit Bus ParameterLibs Report View Op Image: Image	Block Copy Waveforms Choose the Start, End, Place At units Image: Time Clock Cycles Controlling Start: 0 Image: S	? ×	×
RESETN LOAD ENABLE DATA[15:0] AAAA COUNT[15:0]	DATA DATA		
	OK Cancel Help]	



	Block Copy Waveforms	? ×
WaveFormer Lite File Export Edit Bus ParameterLibs Report View Op Image: Image	Choose the Start, End, Place At units	
Diagram - untitled1.btim* Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VÅL Add Clock Add Spacer Hold Text Marker J LOW TRI VÅL 40.00ns 180.0ns Ons 150ns 100ns	Start: 0 ns Insert End: 100 ns Overwrite Place At: 220 ns # of Copies: 1 Change Waveform Destination	_ □ × ▲
CLK CLK <td>DATA DATA :</td> <td></td>	DATA DATA :	
	OK Cancel Help	



🤷 WaveFormer Lite
File Export Edit Bus ParameterLibs Report View Options Window Help
] ☞ 등
☐ Diagram - untitled1.btim*
Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VÅL INVal WHI WLO HEX Q + Q F Add Clock Add Spacer Hold Text Marker
229.0ns 49.00ns Ons 50ns 100ns 150ns 200ns 250ns 300ns 350ns
RESETN
LOAD
ENABLE
DATA[15:0] AAAA (BBBB AAAA
COUNT[15:0]
Copy of waveform is inserted!
Zoom to a specified range Simulation Inactive



 WaveFormer Lite Supports Creation of Analog Stimulus for Fusion FPGAs

🙅 WaveFormer Lite - [Diagram - Top_tbench.btim*]							
🖵 Eile Import/Export Edi	it <u>B</u> us ParameterLibs <u>R</u> eport <u>V</u> iew	Options <u>W</u> indow <u>H</u> elp						_ 8 ×
🗳 🖬 🎒 🏚 🥚	€ € € ® ™ Search		- ∢ _№ ▶ _№	j 🚰				
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample Hold Text Marker → HIGH		HEX Q+ QF	ViewVariables Class Methods				
2.479ms 2.428ms	0us 200us 400us	600us 800us	1.0ms 1.2ms	1.4ms 1.6ms	1.8ms	2.0ms	2.2ms	2.4ms
VAREF								^
RESULT_AV5V[11:0]								
RESULT_TEMP[11:0]								
Volt1								
Volt2								
Volt3								
Volt4								
Volt5								
Volt6								
Volt7								
Volt8								
Volt9								
Volt10								
Volt11								
Volt12								
Volt13								
Volt14								
Volt15								
Volt16								
Volt17								
Volt18								~
< >>	<	Ш						>
Click to draw waveform	n displayed on red state button		Simulation Inactive			INS	Ln: 0	Col: 0



Specify Analog Signal Type

		Signal Properties	
	🙅 WaveFormer Lite - [Diag		
	🕂 Eile Import/Export Edit B	u: Name: Volt1 PActive Low P	_ @ ×
	🖻 🖬 🗿 🏚 🎒 🍳	Simulate Once Analog Props Grid Lines	▼ 4 _M > _M
	Add Signal Add Bus Dela Add Clock Add Spacer Hok	y Orive C Simulate C Watch C Compare U	0 HEX Q - Q R Class Methods
	506.8us 456.4us Du	S Type: Boolean Eqn 💌 ex. (SIG1 and SIG2) delay 5	1.0ms 1.2ms 1.4ms 1.6ms 1.8ms 2.0ms 2.2ms 2.4ms
	VAREF		<u> </u>
	RESULT_AV5V[11:0]	Clock: Unclocked Edge/Level: pos	
	RESULT_TEMP[11:0]	Set: Not Used Clear: Not Used	
	Volt1		
	Volt2	Clock Enable: Not Used <u>Advanced Register</u>	
	Volt3		
	Volt4	Wfm Eqn 8ns=2 (5=1 5=0)*5 9=H 9=L 5=V 5=X	
	Volt5	Label Eqn Ramp(2.5,2.5,900000)	
	Volt6	Export Signal Direction: output	
	Volt7	Analog Display Size Ratio: 1	
Select Te	emperature,	Signal Type: actel_voltage	
Voltage o	r Čurrent —	Radix: real 4_state_vector LSB: 0	
from list		Falling actel_temperature ge Sensitive	
	L Val4121	OK actel_voltage_common / Next —	
	Vulti3		
	Volt14		
	Volt16		
	Volt17		
	Volt18		
	< >> <		×
	State Button: if activated, n	ext segment will be drawn valid	Simulation Inactive INS Ln: 0 Col: 0



Using Built-in Functions

	Signal Properties	X
🙅 WaveFormer Lite - [Diagra		
🕂 Eile Import/Export Edit Bus	Name: Volt1 CActive Lo	~
] 🖻 🖬 🗿 🏚 🎒 🍭	Simulate Once Analog Props Grid Lines	······································
Add Signal Add Bus Delay Add Clock Add Spacer Hold	Orive C Simulate C Watch C Compary Equation Entry Verilog VHDL	e HEX Q F View Variables
506.8us 456.4us Ous	Type: Boolean Eqn 💌 ex. (SIG1 and SIG2) delay 5	5 1.0ms 1.2ms 1.4ms 1.6ms 1.8ms 2.0ms 2.2ms 2.4ms
VAREF		
RESULT_AV5V[11:0]	Clock: Unclocked 💌 Edge/Level: pos 💌	
RESULT_TEMP[11:0]	Set: Not Lised V Clear: Not Lised V	
Volt1		Click to select list of signal functio
Volt2	Clock Enable: Not Used 💌 Advanced Register	
Volt3		
∨olt4	Wfm Eqn 8ns=Z (5=1 5=0)*5 9=H 9=L 5=V 5=X	
Volt5	Label Eqn Ramp(2.5,2.5,900000)	
Volt6		,(Concatenate)
Volt7	Analog Display	Dec(start, decrement, count)
Volt8		IncString("string", start, increment, count)
Volt9	Signal Type: actel_voltage	Range(start, finish, count) RandInt(count, Range, to zero)
Volt10	Radix: real 💽 Bus MSB: LSB: 0	Hex(list)
Volt11	🗖 Falling Edge Sensitive 🔲 Rising Edge Sensitive	Bin(list) Ren/(list_count)
Volt12	OK Cancel Apply Prev Next	Skip(count)
Volt13		File("filename.txt")
Volt14		Map{operations} list
Volt15		PRBS7(length, seed)
Volt16		PRBS15(length, seed) Sin(amplitudeV, period, duration)
Volt17		SinStart(amplitudeV, period, duration)
Volt18		SinEnd(amplitudeV, period, duration)
x		CapDischarge(amplitudeV, RC, duration)
State Button: if activated nex	xt seament will be drawn valid	Ramp(StartV, EndV, Duration)
	a segment will be allown valia	



Analog Stimulus

🙅 WaveFormer Lite - []	Diagram - Top_tbench.bti	m*]					
🕂 Eile Import/Export Edi	it <u>B</u> us Parameter <u>L</u> ibs <u>R</u> eport	: <u>V</u> iew <u>O</u> ptions <u>W</u> indow <u>H</u> elp					_ @ ×
🛎 🛛 🖉 🏚 🍊		earch	▼ 4 ₈ > ₈₀	V			
Add Signal Add Bus Add Clock Add Spacer	Delay Setup Sample HIGH LG		HEX Q + Q F Image: Comparison of the second secon	ViewVariables Class Methods			
73.71us 23.33us	0us 200us 400	us 600us 800us	1.0ms 1.2ms	1.4ms 1.6ms	1.8ms 2	2.0ms 2.2r	ns 2.4ms
VAREF							~
RESULT_AV5V[11:0]							
RESULT_TEMP[11:0]							
Volt1	<u>) to xo xo</u>	0 p.zsp.5p.rs(1) uzs(1.5) rs(2) p.zsp.f	j2.5k.+7q2.+5k.+2q2.4k.37q2.35j	23282.3,2279225,2.5,2.5	<u> 2.5 2.5 2.5 </u>	<u>2.5 (2.5 (2.5 (</u>	2.5 (2.5 (2.5
Volt2							
Volt3							
Volt4							
Volt5							
Volt6							
Volt7							
Volt8							
Volt9							
Volt10							
Volt11							
Volt12							
Volt13							
Volt14							
Volt15							
Volt16							
Volt17							
Volt18							~
< >	<						>
Click to draw waveform	n displaved on red state bu	itton	Simulation Inactive			INS L	.n: 0 Col: 0



Saving Stimulus

Save Stimulus

File > Save

- File Name May Contain Name of Top-level Module
- Stimulus Appears on Libero File Manager Tab





Generating the Testbench

- Select Export from WaveFormer Lite Menu
 - WaveFormer Lite Has Many Export Options
 - Recommendations
 - VHDL Testbench Select "VHDL with Top Level Testbench"
 - Verilog Testbench Select "Verilog with Top Level Testbench"




Waveform and Testbench





Design Verification with ModelSim AE





ModelSim AE, PE, LE, & SE

	Actel Edition	PE	LE	SE
Operating System	Windows	Windows	Linux	All
Advanced Optimizations	N/A	N/A	N/A	Included
Performance Analyzer	N/A	N/A	N/A	Included
C Debugger	N/A	N/A	N/A	Included
Dataflow Window	N/A	Optional	Included	Included
Waveform Comparison	N/A	Optional	Included	Included
SWIFT	N/A	Optional	Optional	Included
Code Coverage	N/A	Optional	Optional	Included
Stand-Alone Viewer	N/A	Optional	Optional	Included
Assertions (PSL)	N/A	Optional	Optional	Optional
SystemC	N/A	Optional	Optional	Optional



ModelSim AE

- Same Functionality as ModelSim PE
 - Windows XP and Windows Vista Business
 - Node Locked
- Reduced Performance
 - ~ 30% of ModelSim PE Performance
- Single Language
 - No co-simulation (VHDL and Verilog) capability
- Structural Simulation Limited to Actel's Gate-level Libraries
 - Pre-compiled libraries required
- Supported Through the Actel



ModelSim Default Window Layout





ModelSim Dockable Windows

- Windows Within The Main Window Are Dockable
 - Move The "Drag Handle" To The Desired Location



- Additional Window Features
 - Drag & Drop
 - HDL Items Can Be Dragged from Dataflow, List, Signals, Source, Structure, Variables, and Wave Windows ...
 - ... And Dropped into either List or Wave Window
 - Automatic Window Updating



Common Window Features

Drag & Drop

- The HDL items can be dragged from the Dataflow, List, Signals, Source, Structure, Variables, and Wave windows and dropped into the List or Wave window
- Automatic window updating
 - Dataflow, Process and Objects windows
- Find Feature
- Sorting HDL items
 - Sort ascending, descending or appearance order
 - Process, Signals, Source, Structure, Variables and Wave windows
- Combining Items



ModelSim Main Window

Main Window Appears when ModelSim is Launched





ModelSim Main Window Active Project with Design Loaded



ModelSim> prompt before design is loaded. **VSIM>** prompt is displayed after design is loaded



delta time step, environment)

ModelSim Toolbar





Workspace Window

- Workspace Provides Access to:
 - Libraries
 - Compiled Design Units
 - Design Source Files
 - Memory Modules

🖬 Workspace				×
Workspace	e :		今 世	1 X
▼ Name		Туре	Path	-
	ision	Library	D:/Libero7.3/Model/actel/Vhdl/fusior	
De 👖 P	resynth	Library	presynth	
E	analoo2	Entity	D:/Actelprj/Fusion_applications/Cory	
⊡Ē	Simulate	Entity	D:/Actelprj/Fusion_applications/Cory_	
I ⊡Ē	Simulate with Coverage	Entity	D:/Actelprj/Fusion_applications/Cory_	
I ⊡Ē	Edit	Entity	D:/Actelprj/Throughput7.3/smartgen/	
I ⊡Ē	Refresh	Entity	D:/Actelprj/Throughput7.3/smartgen/	
I ⊡Ē	Recompile	Entity	D:/Actelprj/Throughput7.3/smartgen/	
I ⊡Ē	Optimize	Entity	D:/Actelprj/Throughput7.3/smartgen/	
I ⊡Ē	Update	Entity	D:/Actelprj/Throughput7.3/smartgen/	
∎ ⊡Ē	Create Wave	Entity	D:/Actelprj/Throughput7.3/smartgen/	
∎ ⊡Ē		– Entity	D:/Actelprj/Throughput7.3/smartgen/	
∎ ⊡ Ē	Delete	Entity	D:/Actelprj/Throughput7.3/smartgen/	
∎ ⊡Ē	Copy	Entity	D:/Actelprj/Throughput7.3/smartgen/	
⊡Ē	Сору	– Entity	D:/Actelprj/Throughput7.3/smartgen/	
⊡Ē	New 🕨	Entity	D:/Actelprj/Throughput7.3/smartgen/	
⊡Ē	Properties	Entity	D:/Actelprj/Throughput7.3/smartgen/	
<u>⊕</u> Ē	riopenies	Entity	D:/Actelprj/Throughput7.3/smartgen/	
i 🔂 🕘 🔋	nitcfg_xd	Entity	D:/Actelprj/Throughput7.3/smartgen/	
i 🔂 🕘 🔋	nitcfg_xe	Entity	D:/Actelprj/Throughput7.3/smartgen/	
i 🔂 🕘 🔋	nitcfg_xf	Entity	D:/Actelprj/Throughput7.3/smartgen/	
LAR BUILDERIN PROD			D. M. A. L. OTH	-
<u>-</u>				
Libr,	ary 🛺 sim 🖺 Files 🚦	🚦 Memories		< >



Source Window

- View and Edit HDL source code
 - Color-coded comments, keywords, strings, numbers, executable lines, identifiers, system tasks, text
 - Save, compile and restart simulation from Source window
- Features
 - Describe and Examine selected items
 - Find and Replace items
 - Set Breakpoints

•Blue line numbers - executable lines where a breakpoint can be set

•Red diamonds – enabled breakpoints

•Hollow diamonds – disabled breakpoints

•Blue arrow - denotes a process selected in the Process window





Objects Window

- Shows Names and Values of HDL Items in Current Region Selected in the Workspace
 - Objects include signals, nets, registers, constants and variables not declared in a process, generics and parameters
- Items Can Be Sorted in Ascending, Descending or Declaration Order
- Hierarchy (+) Expandable
 - VHDL Items Signals
 - Verilog Items Nets, Register Variables
 - Named Events
- "Drag & Drop"
 - Wave & List windows
 - Force Apply Stimulus
 - Filter Signal Types (input,output
 - etc)
 - Find HDL Items





Wave Window

- Displays Waveforms of Simulation Results
 - VHDL signals, processes and shared variables
 - Verilog nets, registers, variables and named events
 - Virtuals virtual signals, busses and functions





Wave Window Features

 Drag and Drop from from the List, Process, Signals, Source, Structure, or Variables window

Zoom

control

₿₿⊇⊇|**#**₽Ъ

 $\Theta \Theta \Theta \Theta$

Now: 3 ms. Delta: 3

Add /

Delete

cursor

┺┺┺┹┲┹┺┓

1 💠 📦

Timing Measurements with Multiple Cursors Find cursor transition

File Edit View Add Format Tools Windo

Cursor 2 320000 ns

🔳 wave - default

/testbench/rs lcd

130144605 ps to 335627369 ps

- Display Formatting
 - Dividers
 - Window Panes
- Signal Formatting
 - Radix
 - Combining
- Simulation Control
 - Breakpoints
 - Restart, Run
 - Run length
- Sort
 - Ascending or descending
- Zoom
- Find



🌢 💥 🖉 🖄

Simulation

control

100 ps 💠 트님 트날 💥 (P) (P 🐑 🕦 😷

160000.

Advancing Simulation Time Main and Wave Windows

From Main Window

ModelSim ACTEL 5.6b - Custom Actel Version

File Edit View Compile Simulate Tools Window

- At the VSIM prompt:
 - VSIM 12> run 100 ms
- In The Main Window Tool Bar:

Help

•Run - run the current simulation for the specified run length
•Continue Run - continue the current simulation run until the end of the specified run length or until it hits a breakpoint or specified break event
•Run - All - run the current simulation forever, or until it hits a breakpoint or specified break point or specified break event



- 🗆 ×



Actel Corporation Confidential © 2009



Restarting Simulation

Restart to Zero

- At the VSIM prompt force a re-start
 - VSIM 12> restart -f
- In The Main Window Run > Restart or Restart Button
 - Will display restart dialog.

Restart Dialog

- Keep current
 - Listed Signals
 - Waved Signals
 - Breakpoints
 - Logged Signals
 - Virtual Signals

М	Restart 📃 🗆 🗙				
	Кеер:				
	List Format				
	🔽 Wave Format				
	✓ Breakpoints				
	Logged Signals				
	Virtual Definitions				
	<u>R</u> estart <u>C</u> ancel				





🔢 wave - default	
<u>File E</u> dit <u>V</u> iew <u>A</u> dd F <u>o</u> rmat <u>T</u> ools <u>W</u> indow	
┃ 🗅 • 😹 🖬 🍏 🥔 🐰 🖻 🛍 😂 😂 🖊 🖿 🎕	▙ <mark>▙▙॒▙₹₣₹₩₽₩</mark> ₩₩ <u>₩</u> ₩ ₩ ₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩₩
1 ← 🛶 EF 100 ps 븆 EL EL EL M ?)	₽₽₽₩₩₽₽ €€€€\$
Messages	
<pre>/testbench/clk 1 /testbench/rs_lcd 1 /testbench/rs_lcd 0000 /testbench/en_lcd 0 /testbench/r_nw_lcd 0 /testbench/sw1 0 /testbench/sw4 1 /testbench/sw5 1</pre>	
<pre>cc_instance/;state[u]_net_1\ 0</pre>	
Now 450000 ns	
0 ps to 472500 ns Now: 450 us Delta: 3	



📰 wave - default	
<u> Eile Edit View A</u> dd F <u>o</u> rmat <u>T</u> ools <u>W</u> indow	
┃ 🗋 • 🖨 🖬 🍏 🎒 👗 🖻 🛍 😂 😂 🖊	SEB LLTT ■ ■ 1 ■ 1 = 5 S S S S
🛧 ┿ 👍 🚺 100 ps 븆 🖳 💱 😫 🕅	1 권 한 안 1 1 1 Combine Selected Signals 🔀 🎢
Messages	Result Name
/testbench/clk 1 /testbench/rs_lcd 1	
+- /testbench/data_lcd 0000 /testbench/en_lcd 0 /testbench/r_nw_lcd 0 /testbench/sw1 0 /testbench/sw4 1 /testbench/sw5	Order to combine selected items Image: Content of Result Indexes Image: Content of Resu
Icd_instance/\state[6]_net_1\ 0 Icd_instance/\state[7]_net_1\ 0 Icd_instance/\state[8]_net_1\ 0	Image: Second
Now 450 Image: Construction of the second sec	000 ns 1 ns 100000 ns 200000 ns 300000 ns 400000 ns ↓ Delta: 3 1



📕 wave - default			X
<u>File E</u> dit <u>V</u> iew <u>A</u> dd F <u>o</u> rmat <u>T</u> ools	<u>W</u> indow		
] 🗋 • 🚅 🖬 🍏 🎒 👗 🖻 🛍	요리 # 문 많 분 분 분	. ★ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$	ď
🛛 🛧 ┿ 🕴 📑 🗍 100 ps 븆 🗉	👥 👥 🕄 (6) 🕅 😫 💷	Combine Selected Signals	
Messages		Result Name	
<pre>/testbench/clk /testbench/rs_lcd</pre>	1	Control_FSM	-
<pre> +- /testbench/data_lcd /testbench/en_lcd /testbench/en_lcd /testbench/sw1 /testbench/sw4 /testbench/sw5 lcd_instance/\state[0]_net_1\ /cd_instance/\state[1]_net_1\ /cd_instance/\state[2]_net_1\ /cd_instance/\state[3]_net_1\ /cd_instance/\state[3]_net_1\ /cd_instance/\state[3]_net_1\ /cd_instance/\state[5]_net_1\ /cd_instance/\st</pre>		Order to combine selected items))0000 I op down ● Bottom up) Order of Result Indexes) ● Ascending ● Descending) I Reverse bit order of bus items in result) I Flatten arrays)	
<pre></pre>	0 0 0 0	Flatten records OK Cancel	
Now 0 ps to 472500 ns	450000 ns 0 ns	100000 ns 200000 ns 300000 ns 400000 ns	



🔢 wave - default	
<u>File E</u> dit <u>V</u> iew <u>A</u> dd F <u>o</u> rmat <u>T</u> ools <u>W</u> indow	
│ 🗋 • 😅 🖬 🦈 🚭 │ 🐰 🖻 🛍 🏠 😫 │ 🖊 🖿 『	▙ <mark>▏<mark>ᅶ</mark>╘┶╼┋╤╤┋<mark>╞╺╔╔┇╡</mark>┠<mark>╻╻╻</mark>┇<mark>╻</mark>╻╻╻╻ ┢</mark>
▲ 🛶 🛛 🗄 🚺 100 ps 븆 🚉 💱 👬	፻• ፻• 🌇 🧐 😍 🔍 🔍 🔍 💽 💽 🔝 🕅 >+ ∰
Messages	
/testbench/clk 1 /testbench/rs_lcd 1 /testbench/data_lcd 0000 /testbench/en_lcd 0 /testbench/r_nw_lcd 0	
√ /cestbench/swi 0 √ /testbench/sw4 1 ↓ /testbench/sw5 1 ①	
Now 450000 ns	0 ns 100000 ns 200000 ns 300000 ns 400000 ns
K F K F	
0 ps to 472500 ns Now: 450 us Delta: 3	0



Wave Window Saving Wave Data

- Signals Added to Wave Window can be Saved
 - File > Save from Wave window
- Select Saved Wave Format in Libero Simulation Options for Future Simulation Runs





Wave Window Saving Wave Data (cont.)

- Enter File Name in Save Format Dialog box
 - Enter name on Libero simulation tab to include signals in future simulation runs

	M Save Format	
Enter file name \longrightarrow	D:/Actelpri/Fusion_labs/data_storage/simulation/wave.do	rowse
	Save contents	
	<u> </u>	ancel



ModelSim Macro Files

- ModelSim Commands can be Saved in a Macro File
 - The do command executes commands.
 - A macro file can have any name and extension.
- Command line Syntax:
 - do<filename> [<parameter_value>]
 - Example: do run.do
- Macros can also be run from the Main Window Toolbar
 - Tools > Execute Macro

```
vlib presynth
vmap presynth ./presynth
vcom -93 -work presynth D:/Actelprj/count32/hdl/count32.vhd
vcom -93 -work presynth D:/Actelprj/count32/stimulus/count32.vhd
vsim presynth.testbench
add wave /testbench/*
run 1000ns
```



Libero Simulation Options ModelSim Do File Options

- Simulation Options Can Be Set from Simulation Tab
 - Select Project > Options
 - Results Saved in run.do File

Use Automatic Do File: Libero sets simulation options automatically





Libero Simulation Options User run.do File





Libero Simulation Options Waveform Options

Specify Signals to be Displayed in ModelSim Wave Window

Project Settings		
Device Flow Simulation		
ModelSim options	Name	Value
Waveforms	Include DO File	
Usim command	Included DO File	./wave.do 🔜
ProASIC3	Display waveforms for	top_level testbench
	Log all signals in the design	ম
		Default
P	ОК	Cancel Help





Libero Simulation Options ModelSim VSIM Commands

 Specify Simulator Resolution and Post-Layout Simulation Operating Conditions





Invoking ModelSim Pre- or Post-Synthesis

Click "Simulation" Project Flow Window or …





Associating Stimulus

- Libero Prompts for Testbench if none is Associated
 - Select testbench from Organize Stimulus dialog





Associating Stimulus Manually

Select a Different Testbench for Simulation





Pre-Synthesis Simulation

- ModelSim Automatically Compiles Design and Runs Simulation
 - Default run time is 1 μS
 - (External) Signals from Testbench Automatically Added to Wave Window
 - Additional (Internal) Signals Can Be Added by User







Simulating Designs Summary

- Capture Design
 - Generate RTL Netlist (VHDL or Verilog)

OR

- Create Schematic
 - May Include RTL blocks
 - Structural VHDL or Verilog Netlist Automatically Created before Simulation
- Create Testbench
 - Use WaveFormer Lite, or Text Editor
- Associate Stimulus
- Run Pre-Synthesis Simulation



Hands-on Lab 3

- Complete Lab 3 in the Lab Guide
 - Perform Pre-synthesis Design Simulation
 - Save Your Work









Invoking Synplicity

Click "Synthesis" in Project Flow Window or ...


Synplify Interface





Synplify Pro Interface





Result File

- Synplicity Produces an EDIF Netlist
 - <design>.edn
- Libero Automatically Produces Structural VHDL or Verilog Netlist
 - <design>.vhd or <design>.v
 - Results Appear on Files Tab under Synthesis Files





Setting the Target Options

Result File	
Change D:\Actelprj\Bootcamp_stuff\FifoDemo\synthesis\fil	fodemo.edn
Target	
Change Actel eX : EX64 : Std	
ions for implementation: example2_syn : hdl	×
evice Options Constraints Implementation Results Timing Report VHDL	I Implementations:
Technology: Part: Speed:	hd
Actel eX 💽 EX64 💽 Sta	
Device Mapping Options	
Option Value	
Fanout Guide	
Hard limit to Fanout	
Dation Description	
Click on an option for a description.	
	Synplicity

High fanout = slow, small designs Low fanout = fast, large designs Use defaults for first pass

 By default, Synplify will insert Actel I/O macros on all the HDL I/O ports.
 When synthesizing lower-level blocks, this must be disabled.



Global Constraints

- Frequency
- Symbolic FSM Compiler
- Configure HDL Compiler
- Resource Sharing



Global Frequency

Global clock frequency is applied to all clock domains in the design Low value means optimize for area





Symbolic FSM Compiler

📆 Unsaved Project *	
Source Files Add Change Edit Result File Change sw_top.edn Change Source Files work bcd_clk.vhd [VHDL] work bcd_clk.vhd [VHDL] work bcd_cntr.vhd [VHDL] work sw_top.vhd [VHDL] Frequency (MHz) Symbolic FSM Compiler Resource Sharing	When checked Synplify identifies state machined in design and sets encoding
Change Actel 3200DX, part: A3265DX, speed grade: Std, Fanout Limit: 16	Encoding method can be set on
BUN View Log Ready	individual state machines with syn_encoding attribute in the HDL code



State Machine Encoding (VHDL)

Options > Configure VHDL Compiler

Sets the default encoding style for enumerated types

Options for implementation: example2_syn : hdl	1
Device Options Constraints Implementation Results Timing Report VHDL Top Level Entity: Implementations: Implementations:	C a
Default Enum Encoding:	S C
default onehot : Process/Block boundaries: gray sequential	H
Synplicity	
OK Cancel Help	

Override encoding style on an individual basis using syn_encoding directive in constraint editor or the HDL source code

# of states	default encoding
1 - 4	sequential
5 - 24	one-hot
> 24	gray



Resource Sharing

 When enabled, Synplify performs automatic sharing of operator resources, including adders, subtractors, incrementers, and decrementers.







With resource sharing

Without resource sharing



Performing Synthesis

Compile only or check syntax

	-												
Synplify - [D:\Actelprj\EXAMPLE_DESIGNS\EX_Desigpr'\Pure_VHDL_Tut\example2\hdl\example2_syn.prj]	- <u> </u>												
Eile Edit View Project Run HD Analyst Opticals Window Help	. 8 ×												
$P \stackrel{\text{Synthesize}}{\blacksquare} P \stackrel{\text{Synthesize}}{\frown} P \stackrel{\text{Synthesize}}{\frown$	D S												
Syntax Check Shift+F7 Synthesis Check Shift+F8													
Bun TCL Script Job Status Source File Synplicity													
Add D:\Actelpriv Next Error F5 DL hdl Image: Big and the state of the sta													
Change whd who who was a set of the set of t													
Edit Resource Sharing	2												
Resource Sharing Resource Sharing Resource Sharing View Log													



Synplify Log File



- Synplify Log Contains Valuable Information:
 - Warnings and Errors
 - Double-click and Jump to Code!
 - Fanout Limit
 - Extraction Information (Found Counter, FSM, Adder, etc.)
 - Net Loading
 - Logic Buffering and Replication Information
 - Resource Usage
 - Critical Path Timing Analysis



Reading the Log File *Errors*

ViewLoa	💳 strobe.srr (log)	
THOM EOG	🖇 Start of Compile	
	#Sat Feb 27 08:15:48 1999	-
	Synplify VHDL Compiler, version 5.0.8, built Dec 22 1998	
	Copyright (C) 1994-1998, Synplicity Inc. All Rights Reserved	
	<pre>@E:"c:\test\design_definition\hdl\vhdl\strobe.vhd":7:0:7:2 Expec</pre>	ting ;
Λ	l errog parsing file c:\test\design_definition\hdl\vhdl\strobe.v	hd
	(CEND	
\mathbb{N}/\mathbb{L}	Process took 0.87 seconds realtime, 0.93 seconds cputime	
		<u>•</u>
< Double		
Click!	\geq /	
V V r		
Ý		



Reading the Log File Errors





Synplify Area Log File

Synplify Area Log Gives Hierarchical Breakdown of Area

Synplify 8.8A1 - Apr 16 2007 - [C:\Actelp	rj\LCD_driver\VHDL\Solu	ıtion\Top\syn	thesis\TC)P_sy 🔳	
📑 Eile Edit View Project Run Analysis HDL-Ana	lyst <u>O</u> ptions <u>W</u> indow Tech-	<u>S</u> upport We <u>b</u>	<u>H</u> elp	_	a x
🗍 P 🛍 🗏 🖩 🎏 🖬 🎒 👗 🖿 🖻 으	# 🛱 😁 🗍 ⊕ €	>│⊠ ⊉ 🗄	: œ	¥ ← → ≯) /) /
Synplif Source Files	ÿ®				
Add C:\Actelprj\LCD_driver\VHDL\S	synthesis	Туре	Modified		
Change Edit Change Change Change Change Change TOP.edn	TOP.srm TOP.srd TOP.srd TOP.sdf TOP.edn TOP.areasrr Stdout.leg	Netlist (Gate) Netlist SDF edif Hierarchical log	13:21:14 13:21:14 13:21:14 13:21:14 13:21:14 13:21:14 13:02:02	07-Aug-2007 07-Aug-2007 07-Aug-2007 07-Aug-2007 07-Aug-2007 06-Nov-2007	
Target Change Actel ProASIC3 : A3P250 : -2,	run_prop_extract, maxfan	: 12, globalth	reshold: 5	0,	
RUN	^{riew Log} Cancel	dy			
TOP_syn.prj 🖺 TOP.areasrr					
				NUM	



Synplify Area Log File

S Synplii	iy 8.8A	1 - Apr	162	007 - [s	ynthesis\T	OP.areas	rr (cs	v)]							
E Eile E	dit <u>V</u> iew	Project	<u>R</u> un	A <u>n</u> alysis	HDL- <u>A</u> nalyst	: <u>O</u> ptions	<u>W</u> indo	ow Tech- <u>S</u> up	port	We <u>b</u> Hel	P			_ 4	7 ×
🛛 P 🛍 🖡		🖻 🖬	Ø	* 🖻	622	M 🖾	1 🕑	⊕⊅		\$ ₩	ାପ 🕸 🖛	⇒ ¢	ø	<i>p</i>)	D P
0001															
0002	Repor	t for	cel	1 TOP.	def_arch			C-11							
0003						cell		count	usag	area	count*a	area			
0005						CLKINT		1		0.0	0.0				
0006					Data	to ICE		8		1.0	8.U 75.0				
0008					Data_	GNE		1		0.0	0.0				
0009						INBUF		4		0.0	0.0				
0010						MX2 NOR2A		1		1.0	1.0				
0012						OUTBUF		7		0.0	0.0				
0013					RIPPI	LE_CNTR		1		46.0	46.0				
0014						UCU MORT FROM		1		U.U 0 0	U.U 0 0				
0015					,	my_PROH		1		0.0	0.0				
0017					TOTA	AL		32			136.0				
0018	Repor	t for	cel	 1 ատ F	ROM netl	 i st									
0020	Kepor	Instar	ice ;	path:	FROM_ins	stance									
0021								Cell	usaș	ge:					
0022						Cell		count 1		area 0 0	count*a	area			
0023						UFROMH		1		0.0	0.0				
0025						VCC		1		0.0	0.0				
0026					тоти	ΔТ		з			0 0				
0028															
0029	Repor	t for	cel	l Data	_to_LCD.1	netlist									
0030		instar	ice	path:	icd_inst	tance		Cell	usad	Je ·					
0032						cell		count	acco	area	count*a	area			
0033						AO1E		1		1.0	1.0				
0034						AU1D AX1F		2		1.0	2.0				
0036						AX1C		ĭ		1.0	1.0				
0037						AX1E		1		1.0	1.0				ا کے
]							_							<u>1</u>
								Li	ne 1,	Col 1				NUM	
📑 TOP	_syn.prj	🖹 TOP	.areas	n j											
													Ν	UM	



Synplify Constraint Editor (SCOPE)

Synplify 9.4A1 - [C:/Actelprj/find_min/synthesis/find_min_syn.prj]	
🐉 🛅 Eile Edit View Project Import IP Run Analysis HDL-Analyst Options Window Tech-Support Web Help	-8×
8 🔅 🏵 🗊 🚱 😣 🚱 🔦 D 🖏 🖓 🖓 🖓 🖓 🖓 🕲 🕼 😸 🕼 😳	뿔 (구 다) Q, Q, Q, »
Add Change Edit Source Files VHDL VHDL Synthesis Synthesis Synthesis VHDL Find_min_syn.pri VH2 bytes	Synplicity* Simply Better Results Frequency (MHz) 100 Symbolic FSM Compiler Resource Sharing
Result File	1
Change C:\Actelpr]\find_min\synthesis\find_min.edn	
Target	
Change Actel ProASIC3 : A3P250 : VQFP100 : -2	
RUN View Log Cancel	
B find_min_syn.prj	

- Synplify and Synplify Pro Include a Spreadsheet-like Constraint Editor
- Extremely Easy to Use



Synplify Constraint Editor (SCOPE)

S Synp	lify	9.4A1 -	[C:/Actel	prj/find_n	nin/sy	nthesis/	find_min_	syn.prj]							
🕑 🗗	File	e Edit Vie	w Project	Import IP	Run	Analysis	HDL-Analyst	: Options	Window	Tech-Supp	ort We	b Help			- F ×
i 😰 🔹	D	New								(Itrl+N	の時間	\$	-> Q, D,	🔍 »
0 5	C	Open								(Itrl+O				
		Close													
		Save								(Itrl+S				
	a	Save As													
		Print								(Sy	n <i>plicit</i> y)"
		Print Setup)												
Ad		Print Imag	e										Simpl	y Better Result	s
Char		Build Proje	ct										Freque	ncy (MHz)	
Edi	B	Open Proje	ect									2 bytes	100		-
		New Proje	:t										Symbo	lic ESM Comp	iler 🖌
		New Work	space										- Synnbo		
		Close Proje	ect										1	Resource Shar	ing 🗹
		Recent Pro	njects								•				
		1 C:\Actelp	orj\Cortex-P	11AF5_Jab\V 41AE5_Jab\W	HDL\M1 svilee\M	AFS_SOC	(synthesis),50 Claunthosis) ta	C_TOP_syr	1_1.s	New				?	
		3 Cr)Actelr	ri)Cortex-P	41AFS_lab\₩ 41AES_lab\₩	erilog\M erilog\M	11AF5_50	C(synthesis)S	νμ_sγn_i.s ΟΓ ΤΟΡ sα	ic sde ^{Fi}	ile <u>T</u> ype:					
		4 C:\Actel	ori\Cortex-M	11AFS lab\W	erilog\M	11AFS_SO	C\simulation\t	opons	dc l	Project F	ile (Proje	ct)		ОК	1
		5 C:\Actel	orj\CoreABC	 Fusion_lab		- Solution\C	oreABC_lab\s	/nthesis\ror	n.infc	🙀 Verilog Fi	le				1
		6 C:\Actelp	orj\CoreABC	_Fusion_lab	VHDL\	CoreABC_I	ab\synthesis\	Top_syn_1.	sdc	🚹 VHDL File	•			Cancel	J
		7 C:\Actelp	orj\CoreABC	_PA3_lab\Sc	olutions	\Verilog\Co	oreABC_lab\sy	nthesis\CC/	REAE	Tcl Script					
Char		8 C:\Actelp	orj\CoreABC	_PA3_lab\C	oreABC	_lab\synth	nesis\COREAB	C_TOP_SYM	i_1.5	🛃 Xilinx Opl	tions File			Help]
	_	9 d:\actelp	rj\q3_08_c	ertification\w	eiss\dv	v_cert08\h	idl\top.vhd			Constrai	nt File (Si Desian C	cope) onstraints			-
		Exit								😟 Design P	lan				
			RUN				Re	ady							
						Cancel			l						
B to t									— R	Add To Pro	iect				
🥲 find_	min	_syn.pr)							— Fi	ile Names:					5
									r	-					ן 🛃 🖉
									Fi	ile <u>L</u> ocation:					
									0	C:\Actelprj\C	ortex-M1	AFS_lab\VHDL\M1	AFS_SOC\s	nthesis\]
									E	ull <u>P</u> ath:					
										C:\Actelprj\C	ortex-M1	AFS_lab\VHDL\M1	AFS_SOC\s	/nthesis\]

- Select File >New
- Select Constraint File (Spreadsheet)
 Select Files of type Constraint Files
- Press OK



s: B	ynplify File	9.4A1 - [C Edit View	C: Watelp	rj\find Import	l_mir	Nsynthe	e <mark>sis\f</mark> i	nd_n	nin_s nalvst	yn_1.s	dc *] Win	dow	Tech-9	5uppo	rt Web	Help				(3 ×
	* •			I &	D	D	A		5	,	(50)		롰	•	D 3		÷	0 \$	4		Ð, (Э,	»
:	()>	I P F		₩ 18		53																	
	Enabled	Cl	ock Object						Clock	Alias					requent (MHz)	Perio (ns)	d	Clock	Group	Rise / (ns)	4t	F	
1	•	mclk													100	10		default_c	lkgroup_	0			
2																							
3																							
4																							
5																							
6																							
7																							
8																							
9																							
1																							
1																							
1:	2																						
1	3																						
1	•																					_ -	
	[tealus [] c			10.1						••••					- 1			ou!			•		
	find min s	lock to Cloc	K Input	s/Outpu	.sdc *	Registers	; D	elay Pa	aths	Attribu	tes	1/0 5	otandar	rds	Compile	Points	(Other					
			_		1	, K														☑ 💷.	✓.	Q	
							/	Сс	on	sti	ra	in	†	e	dit	or	1	tab)				

- Constraint Editor tabs Support:
 - Clock Frequency or Period



55	ynplify	9.4A1 - [C:\A	ctelprj\find_m	in\synthesi	s\find_mi	n_syn_1.sc	lc *]								
1	🗊 Eile	<u>E</u> dit <u>V</u> iew Pr	oject <u>I</u> mport IP	<u>R</u> un A <u>n</u> alysi	s HDL- <u>A</u> nal	yst <u>O</u> ptions	<u>Wi</u> ndow T	ech-Syppoi	rt We <u>b H</u> el	Þ					ð×
8	1	1 🔲 🙆 🖁	I 🗿 🔦 🗅	P 🖓	<u>∩</u> (∆ (A 🗭 🗭	۲	토 😔	D X	5 J	ŝ	¢ 4) Q,	⊕, 6	s »
2	-=+ -=+			° 8											
	Enabled	From Clock Ed	lge To Clock Edg	e Delay	False				Comment						P
1				(15)							_	_	_	_	11
2															
3	1														
4	1														
5															
6															
7															
8															
9															
10															
11															
12															
13															
14															
15 Cl	ocks (l Clock to Clock	Inputs/Outputs	Registers	Delay Path	ns Attribut	es I/O Sta	andards	Compile Poin	ts Othe	ər				
P	ind min :	syn.pri 🔳 fir	nd min syn 1.sdc	*											
													I	. 🖌 🔊	

- Constraint Editor tabs Support:
 - Clock Frequency or Period
 - Clock to Clock timing



5	Sy	nplify 9	.4A1 - [C:\Actelp	rj\find_min\synthesis\f	ind_min_s	yn_1.sd	c *]								
B	F	ji File	<u>E</u> dit <u>Vi</u> ew <u>P</u> roject	Import IP Run Analysis	HDL- <u>A</u> nalyst	Options	<u>Wi</u> ndow	Tech-Syppo	rt We <u>b</u> <u>H</u>	elp				-	Ð×
: 6	Ç	\$	🔲 🙋 📓 👹	N 🔦 D 🖻 🛯 🖓	₩ 🕅	ø 🙍	۵ 🌑	류 🗄 🏵	D	影:3	1	$\langle \Rightarrow \Rightarrow \rangle$	Ð,	Ð, (∋, »
ļ				a % ⊜ .											
ſ		Enabled	Port	Туре	Clock Edge	Value (ns)	Route (ns)			Comm	ent				P
ľ	1		<input default=""/>	input_delay											
ľ	2		<output default=""></output>	output_delay											
ľ	3	•	STROBEn	input_delay	mclk:r	7.5									
ľ	4	•	A_in[23:0]	input_delay	mclk:r	7.5									
ľ	5	•	B_in[23:0]	input_delay	mclk:r	7.5									
ſ	6	•	C_in[23:0]	input_delay	mclk:r	7.5									
ľ	7	•	D_in[23:0]	input_delay	mclk:r	7.5									
ľ	8	•	DataMin[23:0]	output_delay	mclk:r	2.5									
	9	•	mrst_n	input_delay	melkar	7.5									
	10														
	11														
	12														
	13														
	14														
l	15														◄
Ľ	Clo	cks Cl	ock to Clock Input	s/Outputs Registers D	elay Paths	Attribut	es I/O SI	tandards	Compile Po	ints Oth	er				
ß	Dind_min_syn.prj 🖽 find_min_syn_1.sdc *														
														. ✓ .	

- Clock Frequency or Period
- Clock to Clock timing
- Input/Output Constraints



Ss	ynplify 9	.4A1 - [C:\Actelp	rj\find_min\synthesis\fi	nd_min_:	syn_1.sdc *]	
1	🗊 Eile	<u>E</u> dit <u>V</u> iew Project	Import IP <u>R</u> un A <u>n</u> alysis	HDL- <u>A</u> nalyst	t Options <u>Wi</u> ndow Tech-Sypport Web <u>H</u> elp	.ð×
8	1	🔲 🙆 📓 👸	n 😽 🗇 🕼 🔊 🔊	₩ 🖗		⊜, »
			a & a			_
Γ	Enabled	Register	Туре	Route (ns)	Comment	P
1						
2	1					
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15	1					⊡
	ocks C	lock to Clock Input:	s/Outputs Registers D	elay Paths	Attributes I/O Standards Compile Points Other	
2	find_min_s	yn.prj 🛄 find_min	i_syn_1.sdc *			

- Clock Frequency or Period
- Clock to Clock timing
- Input/Output Constraints
- Register Constraints



SS	ynplify 9	.4A1 - [C:\Actelp	rj\find_min\synthe	esis\find_min_sy	n_1.sdc *]				
1	🗊 Eile	<u>E</u> dit ⊻iew <u>P</u> roject	Import IP <u>R</u> un A <u>n</u> a	lysis HDL- <u>A</u> nalyst	Options <u>W</u> indow Tech-Sypport	We <u>b H</u> elp			
	*	🔲 🙆 📓 🎒	l 🔍 🗇 🗭 🛯) 🙉 🖓 🖗 🕼	🕽 😥 🥹 🕵 🛼 🕢 🗊) <u> </u>	\$ (= -) @, @, @, @, »		
2			¥ :≙ .8 68						
	Enabled	Delay Type	From	То	Through	Start/End Cycles	1ax Delay(ns) Comment		
1									
2									
3									
4									
5									
6									
7									
8									
9									
10									
11									
12									
13									
14									
15							▲ ▼		
C	ocks Cl	ock to Clock Input:	s/Outputs Registers	s Delay Paths	Attributes I/O Standards C	ompile Points Other			
1) find_min_syn.prj 🔠 find_min_syn_1.sdc *								

- Clock Frequency or Period
- Clock to Clock timing
- Input/Output Constraints
- Register Constraints
- Timing Exceptions



Ss	nplify 9	0.4A1 - [C:\Actelpi	rj\find_min\synthesis\fi	nd_min_syn_1.	.sdc *]				
1	🗍 Eile	<u>E</u> dit <u>Vi</u> ew <u>P</u> roject	Import IP <u>R</u> un A <u>n</u> alysis I	HDL- <u>A</u> nalyst Optio	ns <u>W</u> indow Tech	n-Sypport W	e <u>b H</u> elp		_ð×
	\$	🔲 🙆 📓 🎒	n 🕹 🕽 🗱 🔊 🖗	🖓 🕅 🗯	🛢 🎯 🚳 🗖	🕑 🕞	3 # O	\$ 4 4 6	& ⊕, ⊝, »
2			a a a						
	Enabled	Object Type	Object		Attribute		Value	Val Type	Desc
1									
2									
3									
4									
5									
6									
7									
8									
9									
10									
11									
12									
13									
14									
15	1								
	ocks C	lock to Clock Inputs	s/Outputs Registers D	elay Paths Attrit	butes I/O Stand	dards Com	pile Points Othe	r	
	ind min s	vn.ori 🔳 find min	svn 1.sdc *						

- Clock Frequency or Period
- Clock to Clock timing
- Input/Output Constraints
- Register Constraints
- Timing Exceptions
- Synthesis Attributes



Constraint Editor Drag and Drop Interface

S	ynplify	9.4A1 - [C:\Act	elprj\find_r	nin\synthesi:	s\find_min_s	yn_1.sdc *]					
1	🗊 File	Edit View Proje	ect Import IP	Run Analysi	s HDL-Analyst	Options Wir	ndow Tech-Suppo	ort Web Help			_ð×
	1	1 🔲 🙋 📓	<i>i</i> 🖗 🕻) 🖡 🏟 (RTL Technolo	•	坐 🛃 🕃	• ₽ 🕮 🛱	0 2 4	-> Q,	⊕, ⊝, »
2	-=+ -=+			°° 8°	Tisland Tir	ning Analyst					
	Enabled	Object Type		Objec	t Physical /	Analyst	Attribute	Value	Val Type		Desc
1						-					
2											
3											
4											
5											
<u> </u>		-									
1/											
8											
9											
10											
11											
12											
13											
14											
15	1										-
	locks (Clock to Clock Ir	nputs/Outputs	Registers	Delay Paths	Attributes	I/O Standards	Compile Points	Other		
P		. 🖽 🖂		*	·	··					
Dowr	hind_min_s hload avail	able vendor IP from	_min_syn_1.soc	: " Support website	•]		



Constraint Editor Drag and Drop Interface (Cont)

SS	nplify	9.4A1	- [Sh	eet 1 o	f 1 - top	level	(of mo	odule	find_	_min)	(RTL	View)	/f	ind_	min.s	rs]									K
III (ji <u>Fi</u> le	<u>E</u> dit	<u>Vi</u> ew	<u>P</u> roject	Import If	<u>R</u> un	Analy:	sis H	IDL- <u>A</u> na	lyst g	<u>O</u> ptions	<u>Wi</u> ne	wob	Tech-9	iypport	: We	<u>b</u> He	lp						.8(×
8	1	<u>i</u>	0		\$) 6		0	~	1 5) 😥	(sm)		2	•	Ð	T	10- 10+	ů	ŝŝ	$\langle \! \! \! \! \! \rangle$	٩,	€,	Э,	»
		•¤ : P			R	00	53																		
	Clock	cances (is (8) s (25) :k Tree	18)																						
🕑 f	ind_min_	_syn.prj		find_mir	n_syn_1.sc	ic * (🕑 find	l_min.s	srs																_
																							. 🗸 .		



Constraint Editor Drag and Drop Interface (Cont)

Synplify 9.4A1 - [Sheet 1 of 1 - top level (of module find_min) (RTL View)/find_min.srs]		
🕣 🛅 File Edit View Project Import IP Run Analysis HDL-Analyst Options Window Tech-Support Web Help		Ð×
Image: Second state Image: Second state<	⊏> @, ⊕, (ð, »
Cascade Close All Next Previous 1 Project Manager 2 C:/Actelprj/find_min_synthesis/find_min_syn_1.sdc 3 C:/Actelprj/find_min/synthesis/find_min.srs		
10 find min svn.pri III find min svn 1.sdc* 3 find min.srs		



Constraint Editor Drag and Drop Interface (Cont)

Sy Sy	mplify 9	.4A1										
폡	<u>File E</u> di	t <u>Vi</u> ew <u>P</u> rojec	t <u>I</u> mport If	P <u>R</u> un A <u>n</u> alysi	HDL- <u>A</u> nalys	t Options	⊻indow Tecl	h-Sypport	We <u>b</u> He	lp		
	¥ ®	III 🙆 📓	1 🗐 🤻			V 🗭 🗭	۲	📕 🤅 🕙	D 3	6 ¥ 3	动合心	2, 9, 9, »
				8 3 8				104	2010 202			
				C:\Actel	prj\find_mi	in\synthesis	\find_min	_syn_1.s	dc *			
	Enabled	Object Typ	be 🗌	C	bject		Attr	ibute		Value	Val Type	De:
1												
2												
3												
4												
5												-
			ļ	5555. 	1						1	
	ocks C	lock to Clock	Inputs/Out	puts Register	s 🔋 Delay Pa	aths Attrib	ites I/O S	Standards	Compile	Points Ot	her	
•			Shee	et 1 of 1 - top	level (of mo	odule find_	min) (RTL '	View)	/find_mi	n.srs		_ = ×
(H)	Dinsta	ances (18)										<u></u>
Ð	Nets	(25)					_				1.1.	
(±)	Clock	< Tree		Selea	t ins	Tanc	e, po	rt o	or ne	et an	a arag	
				into d	ittrik	outes	tab					
												*
🕑 fi	ind_min_s	yn.prj 🔳 fin	d_min_syn_	1.sdc * 🕣 fi	id_min.srs							
			and the second second									



Synplify Directives and Attributes

Synplicity Directives and Attributes

- Let You Direct Analysis, Optimization, and Mapping of Design during Synthesis
- Attributes Control Mapping Optimizations
 - Attributes Can Be Entered in the Constraint Editor or HDL Source Code
 - Synplify Supports Limited Number of Attributes that Can Be Entered in Attribute Pane of the SCOPE Editor
 - *Most* Attributes Are Entered in your VHDL or Verilog Code
- Directives Control Compiler Optimizations
 - Directives *Must* Be Entered in HDL Source Code



Actel Attribute and Directive Summary

NAME	TYPE	VALUE	DESCRIPTION
		1/0	Enables / disables the resource sharing operators inside a
syn_sharing	D	true / false	module during synthesis
			Specifies that a module or component is a black box with only
		1/0	its interface defined for synthesis. The contents of a black box
syn_black_box	D	true / false	cannot be optimized during synthesis
			Prevents an internal signal from being removed during
syn_keep	D		synthesis and optimization
alspreserve	Α	Boolean	Prevents a net from being removed during Place and Route
		sequential,	
		onehot,	
syn_encoding	Α	gray, safe	Specifies encoding style for state machines
syn_maxfan	А	integer	Controls the maximum fanout or an instance, net or port
		1/0	
syn_noclockbuf	А	true / false	Disables automatic insertion of clock buffers
			Specifies register design technique to apply to a module,
syn_radhardlevel	А	string	architecture or instance
syn_replicate	А	1/0	Disables register replication
		1/0	
syn_insert_buffer	А	true / false	Directs Synplify to use specific I/O pads
			Specifies the mumber of global buffers to be used in a
syn_global_buffers	А	integer	ProASIC3/E, IGLOO/e or Fusion design
			Specifies the implementation to use for an
syn_ram_style	А		inferred RAM

Synplify and Synplify PRO for Actel

- Synplify for Actel is Equivalent to Synplicity's Synplify Product
 - Included in Libero Gold
 - Limited to Actel Products Only
- Synplify Pro AE has Additional Features
 - Included in Libero Platinum
 - Limited to Actel products Only



Synplify Pro Logic Synthesis

- FSM Explorer
- Graphical State Machine Viewer
- Pipelining of Multipliers and ROMs
- Compile Point Creation
- Generic Cross-Probing of Critical Paths
- HDL Analyst®
- STAMP Support
- Multiple Implementations & Workspace Support
- Mixed Language design Entry
- Re-timing





Synplify Pro Powerful Graphical Debugging

Language Sensitive Editor Describe the design functionality

Unique RTL View Analyze a technologyindependent block diagram

Technology View View post-mapped schematic with annotated timing





Bi-directional cross-probing between all views

Synplicity Help

- Synplicity Has Complete On-line Manual
 - Invoked from Help Pulldown or by Pressing F1





Opening Synplify Log Files Libero Project Flow Window

 Synplify Log Files can be Opened from Libero Project Flow Window





Hands-on Lab 4

- Complete Lab 4 in the Lab Guide
 - Synthesize the Design with Synplicity
 - Save your Work


Post-Synthesis Simulation





Post-Synthesis Simulation

- Steps:
 - Synthesize Design with Synplicity
 - Generate EDIF Netlist from Synplicity
 - Libero Automatically Creates Structural VHDL or Verilog Netlist
 - Run Post-synthesis Simulation on Structural Netlist





Post-Synthesis Simulation

- ModelSim Automatically Compiles Structural Netlist Exported from Designer
 - Default simulation run time: 1 uS
 - Structural library mapping handled by Libero
 - Pre-compiled libraries do not require compiling prior to simulation







Agenda

Libero Overview

- Libero Editions and Content
- Libero Installation and Licensing
- Libero Design Flows
- 3rd Party Tools
- Designer Overview
- Programming
- Silicon Explorer
- Reference Material









Open Design for Place & Route

Click on "Place & Route" in Project Flow Window or...





Designer Constraint Files

- Libero Automatically Prompts for Designer Constraint Files
 - Select Timing Constraints and Physical Constraints



Designer Interface



- **Designer Provides** Graphical Flow Manager to Lead Designer through **Design Flow**
- **Completed Tasks** Highlighted
- **Design Flow Steps Listed at**
- **User Tools Grouped Below**



Designer Interface (Legacy Products)



- No MVN, SmartPower or SmartTime
- Timer is used for Timing analysis



Designer TCL Script Support

- Industry-standard Language
 - Tool Command Language
- Launch Multiple Tools from Single Script
- Launch Multiple Design Runs





Running Scripts within Designer

- In File Menu, Click Execute Script File
 - Displays Execute Script Dialog Box

Execute Script	
Script <u>F</u> ile:	— Enter name of script file
Browse	
	Enter arguments to be passed
Arguments:	to script file
Run Cancel Help	
ck Run to execute script	

Tcl Scripts can be Executed from the Command Line:

Example:

d:\Libero\Designer\bin\designer script:my_script



Recording Scripts

- Designer Can Export Tcl Script File that Contains Commands Executed in Current Session
- Exported Tcl Script can be used to ...
 - ... re-Execute Same Commands Interactively or in Batch
 - ... Become More Familiar with Tcl Syntax



Importing Source Files

& Designer - [SOC_TOP.adb*]	
🐻 File View Tools Options Help	
New C	
Save C Save As	trl+5 Design Flow
Execute Script C	
Import Source Files Import Auxiliary Files Audit Settings	Back-Annotate
Export	Layout
Preferences	
1 SOC_TOP.adb 2 D:\Actelprj\\SOC_TOP.adb 3 D:\Actelprj\\impl1\Top.adb 4 D:\Actelprj\\SOC_TOP.adb	Programming File
Exit	Import Source Files
Netlist Viewer PinEditor	Note: the relative order of the same type of files is important. When importing multiple EDIF or VHDL files, the top-level file must be last (at the bottom). Use the Up and Down buttons to specify the relative order of the files.
	Source Files Type Add 1 D:\Core8051s_AFS\Libero_projects\VHDL\SOC_TOP\synthesis\ edn Modify 2 D:\Core8051s_AFS\Libero_projects\VHDL\SOC_TOP\synthesis\ sdc Modify
	4
Import source/netlist files into Designer	✓ Merge PDC file(s) with existing physical constraints ✓ Merge SDC file(s) with existing timing constraints Audit timestamp: Mon Aug 25 15:25:48 2008
	Help OK Cancel

Multiple files can be imported at the same time

Libero sends Netlist and Constraint files to Designer Automatically

Import File types:

File Type	Extension
EDIF	*.ed*
VHDL	*.vhd
Verilog	*.V
Actel ADL Netlist	*.adl
Criticality	*.crt
Timing Constraint	
File	*.sdc
ProASIC Constraint	
File	*.gcf
Physical Design	
Constraint File	*.pdc



Importing Auxiliary Files

& Designer - [SOC_TOP.adb*]	
🐻 File View Tools Options Help	_ 2 >
Open C	
Save C	trl+5 Design Flow
Execute Script C	u+u → 👘 → mu
Import Source Files Import Auxiliary Files Audit Settings	Back-Annotate
Export	Layout
Preferences	
1 SOC_TOP.adb 2 D:\Actelprj\\SOC_TOP.adb 3 D:\Actelprj\\impl1\Top.adb 4 D:\Actelprj\\SOC_TOP.adb	Programming File
Exit	Import Auxiliary Files
Netlist Viewer PinEditor	Auxiliary Files Type Add
	1 Side Modify
×	a b b b c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c c <thc< th=""> <thc< th=""> <thc< th=""> <thc< th=""></thc<></thc<></thc<></thc<>
	9 10 11 Note: to import *.vcd files, go to Smart Power.
Import auxiliary files into Designer	1.
	Help OK Cancel

Optional step to import pin files, timing constraints, etc.

Import Auxiliary files after compile completes

Import File types:

File Type	Extension
Criticality	*.crt
PIN	*.pin
Timing Constraint File	*.sdc
ProASIC Constraint File	*.gcf
Physical Design	
Constraint File	*.pdc
Value Change Dump	*.vcd
Switching Activity	
Intermediate File	*.saif
Design Constraint File	*.dcf



Entering Constraints in Designer

- Option 1 Import Files in Designer
 - Source Files are Passed by Libero Automatically
- Option 2 Import Files in TCL Script
- Option 3 Set All Constraints Directly in Designer
 - Physical PinEdit or IO Attribute Editor
 - Timing SmartTime or Timer



Designer File Auditing

Audit Status
The following files are out-of-date: D:\Actelprj\Q3_07_Certification\Khayat\rev2\cert07\synthesis\top.edn D:\Actelprj\Q3_07_Certification\Khayat\rev2\cert07\synthesis\top_sdc.sdc
< <
Choose one of the following options to proceed: Re-import all source files]
O Do not audit these files for the current design session.
C Adjust <u>a</u> udit settings
Нер ОК

I	udit Se	ttings							×
			Sour	ce File Names	Туре	Audit	Result	Change location	1
	1	D:\Actelpi	rj\Q3_0	7_Certification\Khayat\rev	/2\ edn	N	out-of-date		1
	2	D:\Actelpi	rj\Q3_0	7_Certification\Khayat\rev	/2_sdc		out-of-date	Copy locally	
	Audit tim	estamp:		Mon Aug 13 19:28:21 2	007	Res	et to current date/time]	
	He	P					0	K Cancel	

- Designer Source File Auditing
 Ensures Imported Files Are Current
 - All Imported Source Files Are Dateand Time-stamped
 - Designer Notifies You if File Is Changed
- Audit Settings Can Be Changed (File > Audit Settings)
 - Enable / Disable Auditing
 - Move File to New Location
 - Associate File with Current Date
 and Time



Importing Files into Designer - Summary

- Import the Following Source Files
 - EDIF, VHDL, Verilog Netlists
 - PDC, GCF and SDC Files
 - Source Files Are Audited per User Settings
- Import the Following Auxiliary Files
 - DCF, SDC, PDC, GCF, VCD, and SAIF Files



Designer Compile



- Reads Netlist
- Compiles Design into Actel Database (ADB) File
- Runs Combiner
- Performs Design Rule Checking
- Checks for Netlist Errors (Bad Connections and Fanout Problems)
- Removes Unused Logic (gobble)
- Verifies that Design fits into Selected Device



ProASIC3 Compile Options Globals Management

- Automatically Promote Nets to Globals
- Automatically Demote Global Nets to Regular Routing Resources
 - Each option has an equivalent Tcl Compile command

Compile Options	<u> </u>
Categories Select a category: Physical Design Constraints Globals Management Netlist Optimization Display of Results	Globals Management Automatic Demotion/Promotion
 Show these options every time Compi Help 	le is run.



Constraint File Types by Family

Family	Tim	ning	Physical Placement				Netlist Optimiization	
	SDC	DCF	PDC	PIN	GCF	PDC	GCF	
IGLOO	×		×					
Fusion	×		×			х		
ProASIC3	×		×					
ProASIC <u>PLUS</u>	×				×		×	
ProASIC	×				×		×	
Axcelerator	×		×			×		
еX	×	×		×				
SX-A	×	×		×				
SX		×		×				
MX		×		×				
DX		×		×				
ACT3		×		×				
ACT2/1200XL		×		×				
ACT1		×		×				



ProASIC3 Compile Options Netlist Optimization

Perform Netlist Optimization

- Use I/O Registers
- Delete Buffers and Inverters





Compile Wizard - Die and Package

Device Selection Wizard		
<u>F</u> amily: ProASIC3 <u>D</u> ie	Package	
A3PN125Z A3P250 A3PN250 A3PN250Z M1A3P250 A3P400 A3P600 M1A3P600 A3P1000 M7A3P1000 M1A3P1000	144 FBGA 208 PQFP 256 FBGA 484 FBGA	
Speed: -2	Die voltage:	
Cancel	< <u>B</u> ack <u>N</u> ext >	Help

Select:

- Die
- Package
- Speed Grade
- Die Voltage



Compile Wizard - I/O Attributes

De	vice Selection Wizard - Variations 🛛 🛛 🔀
ſ	Reserve <u>P</u> ins
	Reserve JTAG
	✓ Reserve J_AG test reset
	Reserve probe
l	
[I/O Attributes
	Default I/O standard: LVTTL
	Please use the I/O Attribute Editor or PinEditor to change individual I/O attributes
_	
	Cancel < <u>B</u> ack <u>N</u> ext > Help

- Restrict Pin Usage
 - Reserve JTAG Pins
 - Reserve ActionProbe Pins
- Select Default I/O Standard



Compile Wizard - Operating Conditions

evice	Selectio	n Wizard	- Operating	, Conditio	ns			E
_ Ju	Inction Temp	perature (in	degrees Celsius	;)				
B	ange:		<u>B</u> est:	<u>T</u> ypical	l:	<u>W</u> orst:		
	СОМ	-	0	25		70		
Ve	oltage (in vol	lts)						
	Die V	oltage	Ran	ige	Best	Typical	Worst	
	1.5		СОМ		1.575	1.5	1.425	
'								
	VCCI	Wide						
	Voltage	Range	Ran	ge	Best	Typical	Worst	
	1.5		СОМ		1.6	1.5	1.4	
	1.8		COM		1.9	1.8	1.7	
	2.5	_	COM		2.7	2.5	2.3	
	3.3		СОМ		3.6	3.3	3	
			1		,			

- Select Junction Temperature
 - Commercial (0 70°C)
 - Industrial (-40 85°C)
 - Custom
 - Military (-55 125°C)
 - Mil Devices only
- Select Voltage Range
 - Commercial
 - Industrial
 - Custom
 - Military
 - Mil Devices only
 - Die and I/O Voltage Selections



Operating Conditions Radiation Derating

Radiation Derating for AX-S and SX-S

 Add Radiation Exposure Level for Radiation Derated Timing

Devi	ice Selection Wizar	d - Operating Cor	nditions	×			
	Junction Temperatu	re					
	<u>R</u> ange	<u>B</u> est	<u>T</u> ypical	<u>W</u> orst			
	MIL	-55	25	125			
	-Voltage						
	Range	B <u>e</u> st	Typical	W <u>o</u> rst			
	MIL	2.7	2.5	2.3			
		<u>I</u> /O Best	1/0 Typical	I/O Wor <u>s</u> t			
		3.6	3.3	3			
	Radiaton 0 KRad						
	Cancel	<u>B</u> ack Finis	h	Help			



Designer Netlist Optimization

Netlist Optimization

ProASIC3, Fusion, IGLOO and ProASICPLUS

- Combiner can Remove all Buffers and Inverters from Netlist that Have No Effect on Circuit's Functional Behavior
 - Reduces Overall Size of Design
 - Produces Faster Place and Route Times
 - Takes Advantage of Inverted Inputs of Logic Tiles
- Original Netlist Preserved
 - Removed Cells Back-annotated with Ons Delay in SmartTime



ProASIC3, Fusion, IGLOO - Logic Combining

- Combiner Can Combine VersaTiles Configured as Combinatorial Cells
 - Not Supported for ProASICPLUS





ProASIC3/E, Fusion, IGLOO/e Netlist Optimization Constraint Options

Delete Buffer Tree

 Instructs the Compile command to remove all buffers and inverters from a given net

Syntax:

```
delete_buffer_tree [netname]
```



Designer Status Report ProASIC3/E, Fusion, IGLOO/e Designs

🗏 Status.rpt - WordPad						X	
Eile Edit View Insert Format Help							
D 🚅 🖬 🍯 🖪 🛤 🐰 🖻 🛍	v 🖳						

Status Report							
Netlist Optimization Report							
Optimized macros: - Dangling net drivers: 0 - Buffers: 0 - Inverters: 0 - Tieoff: 0 - Logic combining: 5							
Total macros optimized 5 CMP703: Promoted the net 'clk_internal_c' because the compile option promote_globals is set to ON.							
There were O error(s) and O warning(s) in this design.							
 <u>Actual</u> number of tiles used							
CORE IO (W/ clocks) Differential IO GLOBAL (Chip+Quadrant) PLL RAM/FIFO Low Static ICC FlashROM User JTAG	Used: Used: Used: Used: Used: Used: Used: Used: Used:	149 11 0 2 0 0 0 1 1 0	otal: Total: Total: Total: Total: Total: Total: Total: Total: Total:	6144 151 34 18 1 8 1 1 1	(2.43%) (7.28%) (0.00%) (11.11%) (0.00%) (0.00%) (100.00%) (100.00%) (0.00%)		
Global Information:							
Type Used	Tota	1					
Chip global 2 Quadrant global 0	 6 (3 12 (0	33.33%) D.OO%)	_				



MultiView Navigator

MultiView Navigator

- MultiView Navigator Includes the Following Tools:
 - PinEditor, I/O Attribute Editor, NetlistViewer, and ChipPlanner
- Supported for the following families:
 - IGLOO/e, Fusion, ProASIC3/E, ProASIC3L
- Supports Cross-probing Among Different Designer Tools



Click one of these buttons to open MVN



MultiView Navigator





MultiView Navigator Windows

- Design Window
 - View Design as Logical Blocks, Physical Elements, Ports, Nets, and Regions
- World View Window
 - Shows Position of Current Viewing Window Relative to Chip
- Working Area Shows Current Active Tools
 - Tile or Cascade Active Tools
- Log Window Keeps Running Log of Activity
 - Output Shows All Messages
 - Errors Shows Error Messages
 - Warnings Shows Warning Messages
 - Info Shows Informational Messages
 - Find Window Keeps Result of Find Function for Later Usage



MultiView Navigator Toolbar

- File ->
 - Commit Writes any Changes Made in Editors to Design
 - Prelayout Check Verifies Placement Changes in Editors Are Legal

緧

- Edit ->
 - Undo/Redo Allows User to Undo a Mistake or Redo an Accidental Undo
 - Find Enables Find Interface
- Zoom Controls
 - Zoom Region, Zoom In, Zoom Out, Zoom to Fit
- Assignment Options
 - Place, Unplace, Lock (Fix), Unlock (Unfix)
- Tools Menu
 - ChipPlanner, PinEditor, NetlistViewer, I/O Attribute
- "1 click" commands
 - Commit and Check
 - Lock All
 - Unlock All
 - Un-assign All from Location
 - Un-assign All from Region



8

🔍 🔍 🔍 🖾

+0 +0 🔋

	Edit	View	Logic	Nets	Region	Tools
	Ur	ndo		Ct	:rl+Z	
	Redo			Ctrl+Y		
	Cut			Ctrl+X		
-	Сору			Ct	:rl+⊂	
	Pa	aste		Ct	rl+V	
	Select All			Ctrl+A		
	Fir	nd		Ct	:rl+F	
	Hi Ur Hi	ghlight hhighligi ghlight	ht All Color	01 01 01	:rl+B :rl+Shift+ :rl+R	в
	I/O Bank Settings.			Ct	rl+I	


MultiView Navigator Prelayout Checker

- Infeasible Constraints Identified pre-Layout
 - Overlapping Region Checks
 - Resource Overbooking
 - I/O Technology Checks
- Constraint Checker Runs Automatically when You Commit from MVN
 - Users Can Run DRC Checker from MVN Menu (Tools->DRC)



MultiView Navigator Find / Search

- Search for Instances, Nets or Ports
 - Wildcard (*) Matching
 - Advanced Options Choice of Log Window Pane for Search Results
- Cross-probing from Find Tab to the other Four Windows





Actel Corporation Confidential © 2009

MultiView Navigator Active Lists

- "Enables User To Compile Lists Of Important Resources
 - Instances
 - Nets
 - Macros
 - Regions
- Default Lists
 - Unassigned Instances
 - Unassigned Pins
 - Clock Nets
- Navigate Thru Design To Find Status Of Important Design Resources



MultiView Navigator Viewing Active Lists

Open Default Active Lists from MVN Tools Menu





MultiView Navigator Creating Active Lists

Users Can Create New Active Lists





Netlist Viewer

MultiView Navigator Netlist Viewer

Displays Netlist in Hierarchical Manner

• Explore each Level of Hierarchy and Trace Signals





MultiView Navigator Netlist Viewer (cont.)

- Viewing Options
 - Push, Pop, Jump to Top 🛛 🖻 🖻 🖕

 - Right-click on Net to Follow Net to Other Pages or Net Driver



- Highlight, Highlight Append, un-Highlight, un-Highlight All
- Allows Page Splitting

Allow Page Splitting

 Allows User to Decide if All Elements on that Level Are Shown as Single Page



MultiView Navigator Netlist Viewer (cont.)

- View Pre- and Optimized Netlists for ProASIC3/E, ProASIC^{PLUS} and Axcelerator
 - Pre-optimized Netlist Is Original Hierarchical Netlist
 - Optimized Netlist is Flattened
 - Reflects what other Tools Use (ChipEdit, PinEdit)





MultiView Navigator LogicalCone

- Helps View Critical Portions of Netlist
 - Identify Critical Paths using SmartTime
 - Add this Logic to LogicalCone
 - Incrementally Add / Remove Logic from Cone
 - CrossProbe from / to LogicalCone
 - All NetlistView Features available in LogicalCone
 - LogicalCone Tab in Hierarchy Window
 - LogicalCone Menu Accessible from NetlistViewer
 - Can Simultaneously Create Multiple Cones
 - Set of Macros Can Be Highlighted, then Added to Cone
 - LogicalCone Data No Longer Valid after Recompile



LogicalCone User Interface





LogicalCone





I/O Attribute Editor

MultiView Navigator I/O Attribute Editor

- Input/Output Attribute Editor
 - Select (Varies by Family):
 - I/O Standard
 - I/O Threshold
 - Slew Rate
 - I/O Power-up State
 - Enter Load Capacitance
 - Does Not Change SDF File Generation
- Spreadsheet-like Sort, Copy, Paste

📌 MultiView Navigator [find_min *	*]-[I/O	Attribute E	ditor]			_ 🗆	X
→ Eile Edit View Logic Format	<u>T</u> ools <u>V</u>	<u>M</u> indow <u>H</u> elp)			_ 8	×
] 8 ቆ ⊇⊆ & ?]	Q Q	۹ 🖂 🛛	▶ +⊡ +⊡ ● €]] / // #	0 >	🔀 📲 📗	
		Port Name	Macro Cell	Pin #	Fixed	Output Load	
🖃 🗄 Logical 📃 🔺	1	C_in(15)	ADLIB:IB33	Unassigned			
🕰 🔼 📥 📥 📥	2	C_in(7)	ADLIB:IB33	Unassigned			
	3	B_in(2)	ADLIB:IB33	Unassigned			
	4	B_in(23)	ADLIB:IB33	Unassigned			
- 🗠 A_in_pad[3]	5	B_in(18)	ADLIB:IB33	Unassigned			
- 🖸 A_in_pad[4]	6	C_in(20)	ADLIB:IB33	Unassigned			
- 🖸 A_in_pad[5]	7	A_in(10)	ADLIB:IB33	Unassigned			
	8	A_in(19)	ADLIB:IB33	Unassigned			
	9	DataMin(7)	ADLIB:OB33PH	Unassigned		35	
	10	B_in(12)	ADLIB:IB33	Unassigned			
	11	C_in(4)	ADLIB:IB33	Unassigned			
	12	C_in(19)	ADLIB:IB33	Unassigned			
5. 5. O XK 📖	13	D_in(18)	ADLIB:IB33	Unassigned			
	14	D in(27)	ADLIB:IB33	Unassigned			
		'O:Select Nutput / Erro	ed instances hav rs à Warnings à Info à Fi	e been ass ind 1 /	igned.		
I/O Attribute Editor			E	AM: Da DIE: AP	ANZS PACK	AGE: 208 POEP	1 1



MultiView Navigator I/O Attribute Editor (cont.)

Double click on column to sort display by that column

Hold down CTRL key to select multiple rows

••] I/	O Attribute Edito	r					_	
	💌 I/O Standard	Output Drive (mA)	Slew	Fesistor Pull	Input Delay	Output Load	Use I/O Reg	Hot 🔺
1	LVTTL	24	High	None		35		
2	LVTTL	24	High	None		35		
3	LVTTL	24	High	None		35		
4	LVTTL 💌	24	High	None		35		
5	LVTTL	24	High	None		35		
6	PCI	24	High	None		35		
7		24	High	None		35		
8	LVIIL	24	High	None		35		
9		24	High	None		35		
10		24	High	None		35		
11	LVTTL	24	High	None		35		
12	LVTTL	24	High	None		35		
13	LVTTL	24	High	None		35		
14	LVTTL	24	High	None		35		
15		24	Hiah	None		35		

With multiple rows selected, changing the value of a drop-down item with CTRL key pressed will change the value for all rows



MultiView Navigator Package Pins View

Package Pins View Shows All Pins on Package

🐊 MultiView Navigator [co	cax *]	- [1/0	Attribute	Editor]											PX
	ormat	Tools	<u>W</u> indow	Help										- 1	a ×
	5 Ø	e to		1 1 1 1 1 1	2 0 m 🗈	¥ 🔀 🔫	***								
		Pin #	Port Name	Macro Cell	Eunction	Locked	Dedicated		Bank Name	1/O Standard	Output Drive (mA)	Slow	Resistor Pull	Innut Delay	
🖃 🗄 Logical 🔺	14	H2	· ore name	indere con	IO72PB7F7				Bank7	no otandara					
	15	G5			VCCDA		V								
	16	J1	IN3	ADLIB:INBUF	IO71NB6F6				Bank6	LVTTL			None		
⊕	17	G4			IO70NB6F6			Г	Bank6						
	18	J2			IO71PB6F6			Ē	Bank6						
■ 1: DC_BD31_UD	19	H4			IO70PB6F6			Ē	Bank6						
	20	H3			IO68NB6F6			E	Bank6						
	21	J3			IO68PB6F6			V	Bank6						
	22	K2			IO66NB6F6			Г	Bank6						
	23	K1	OUT8	ADLIB:OUTBUF	IO66PB6F6				Bank6	LVTTL	24	Hig	None		
	24	L2			IO64NB6F6				Bank6						
E TE DC UDEME3	25	L1			IO64PB6F6			•	Bank6						
	26	K3			IO62NB6F6			Г	Bank6						
	27	L3			IO62PB6F6			Г	Bank6						
I → ↓ DC_UDFMEH	28	M1			IO60NB6F6			Г	Bank6						
	29	N1			IO60PB6F6			Γ	Bank6						
⊕~_10	30	L4			VCCDA		v								
E E E E E E E E E E E E E E E E E E E	31	N2			IO59NB5F5				Bank5						
	32	P2			IO59PB5F5				Bank5						
	33	M2			IO57NB5F5				Bank5						
	34	M4			IO56NB5F5				Bank5						
	35	M3			IO57PB5F5				Bank5						
	36	M5			IO56PB5F5				Bank5						
	37	P3	OUT5	ADLIB:OUTBUF	IO55NB5F5				Bank5	LVTTL	24	Hig	None		
	38	N3			IO55PB5F5				Bank5						
	39	P4	OUT2	ADLIB:OUTBUF	IO53NB5F5				Bank5	LVTTL	24	Hig	None		
	40	N4	OUT9	ADLIB:OUTBUF	IO53PB5F5				Bank5	LVTTL	24	Hig	None		
	41	P5	OUT7	ADLIB:OUTBUF	IO52NB5F5/CLK				Bank5	LVTTL	24	Hig	None		
i⊡-12 ID2	42	N5	INCLK	ADLIB:CLKBUF	IO52PB5F5/CLK				Bank5	LVTTL			None		
⊞ 1 ∎ ID3	43	M6			VCCPLH		N								
i ⊡ 104	44	L7			VCOMPLH										~
	<				100011175	ш									>
	H I		Ports λ P	ackage Pins /											
			-n n												
	-			1											
A L				Output	Deculte) Find 1	1									
Pins View					Kesules & fille 1	1					FAM: Axce	elerator	DIE: AX125	PACKAGE: 1	.80 CS



Pin Editor

Pin Assignment Options

- I/O Locations Can Be Assigned as Follows:
 - Automatically by Designer Software during Layout
 - By Importing a Physical Design Constraint (.pdc) File
 - Manually using PinEdit and I/O Attribute Tools in Designer
 - Pin Assignments May Be Exported for Later Use



MultiView Navigator PinEditor

- Graphical Pin Location Editor
 - Drag and Drop Placement of Pins
 - Fix Pin Locations for Subsequent Place and Route Runs
- Flip Display o
 - Enables Assignments as if Looking from Top or Bottom of Chip
- Assign I/O Bank Properties for ProASIC3E, Fusion and IGLOOe
- Pinout Can Be Printed for Documentation





I/O Bank Configuration ProASIC3E, Fusion and IGLOOe





VREF Pin Assignment Axcelerator, ProASIC3E, Fusion and IGLOOe

- Select Package Pin And Click Right Mouse Button
 - Select "Use Pin for VREF"





Designer

Automatic I/O Bank Assignment

- I/O Bank Assigner for Axcelerator, ProASIC3/E, Fusion and IGLOO/e
 - Runs automatically during layout
 - Is available when at least one I/O bank is unassigned
 - Automatically assigns voltages to I/O banks that do not have I/Os assigned
 - Fills them with compatible I/Os
 - Assigns V_{REF} pins if required
 - Respects manual assignment already in place
 - Maintains placement quality and performance
 - No impact on device performance
 - Can be controlled manually from within the MultiView Navigator



Pin Assignment Recommendations

- Enter Design as Completely as Possible
 - Don't Worry about Functionality
- Compile (Ignore Warnings) and Layout
- "Fix"All Pin Assignments Edit > Select All then Edit > Fix
- Send Pin Report to PCB Layout
- Continue Working Out Bugs
 - Future Layouts Will Honor "Fixed" Assignments



Chip Planner

ChipPlanner

- Editing and Floorplanning Support for:
 - Fusion, ProASIC3/E, IGLOO/e, ProASIC3L, ProASIC^{PLUS}, ProASIC, Axcelerator, eX, SX-A and SX-S Families
 - Use ChipEditor for All other Actel FPGA Families
- ChipPlanner Capabilities:
 - Editing
 - Place, Unplace, or Move Logic and I/O
 - View Macro Placements Made during Layout
 - View Net Connections with Ratsnest or Route View
 - View Architectural Boundaries
 - View and Edit Silicon Features, such as I/O Banks
 - View Placement and Routing of Paths when Used with SmartTime
 - Floorplanning
 - Create and Assign Logic or Nets to Regions
 - Cross-probe with Silicon Explorer to Select Probes



ChipPlanner Terminology

- Region
 - Defined sub-Portion of Die
 - Shapes Rectangular or Rectilinear (Union of Rectangles)
 - Types:
 - Empty No Logic Can Be Put into this Region
 - Inclusive Assigned Logic Must Be Put into this Region
 - Other Unassigned Logic Can Be Added to this Region by Layout
 - Exclusive Only Assigned Logic Can Be Put into this Region
 - Not Supported for APA or A500K
- Assign
 - Place Logic into Particular Region or Location
 - Similar to "Place" in ChipEditor
- Lock
 - Finalizes Allocation of Logic in Particular Location
 - Similar to "Fix" in ChipEditor



ChipPlanner Editing and Floorplanning

- Drag Logic or I/O to Desired Location
- ChipPlanner Floorplanning Functions



Regions Can Span Logic, Memory Célls and Mice region



ChipPlanner Empty Region

- Region > Create Empty
 - No Logic Assigned to Empty Regions

😳 ChipPlanner	<u>_ ×</u>
	2 2 2 2
Region: UserRegion0 Type: Empty [1 1, 64 32]	
<u>h ammi amma antan atana atana</u>	đ



ChipPlanner Inclusive Region

- Region > Create Inclusive
 - Assigned Logic Put in Inclusive Region
 - Other Logic May also Be Put in this Region





ChipPlanner Exclusive Region ProASIC3/E, ProASIC3L, Fusion, IGLOO/e

- Region > Create Exclusive
 - Only assigned logic placed in exclusive region





ChipPlanner Quadrant Clock Region ProASIC3/E, ProASIC3L, Fusion, IGLOO/e

- Region > Create QuadrantClock
 - Graphically Assign net to a Quadrant Clock





Quadrant Clock Region PCD Constraint ProASIC3, ProASIC3L, Fusion, IGLOO

- Create Quadrant Clock Regions with PDC Constraint
 - PDC Syntax:
 - assign_quadrant_clock -net netname -quadrant quadrant_clock_region [-fixed value]
 - quadrant_clock_region is UL, UR, LL, LR





ChipPlanner Region Color Control

- Individual Region Color Control
 - Regions Have Different Default Colors Based on Types
 - Can Change Each Region's Default Color
 - Region Colors Saved in .adb File
 - Region Colors Reset to Defaults upon Recompile



ChipPlanner **Region Properties**

- Region > Properties
- Indicates:
 - Region Type
 - Region Width, Heig
 - Region Usage
- Shows Region Defau
 - Default Color Can
- Also Provides Acces Window

Change region color

/pe	🕮 Region Properties 🛛 🔀
idth, Height and Origin	Region name : UserRegion0
sage	Region type: 💿 Inclusive Region color:
on Default Color	C Exclusive C Empty
olor Can be Changed	Region Extents
es Access to Assignment	Origin: (1, 25) Width: 96 Height: 8
	Resource usage:
	Name Usage %
Region size and utilization -	
Assign logic to region	Assignment OK Cancel



ChipPlanner Logic Assignment

- Two Logic Assignment Methods
 - Assignment Window (Region > Assign/Unassign Logic...)
 - Provides Search and Selection Capability
 - Also Available from Region Properties Dialog Box
 - Drag and Drop Logic into Region
- Checkmark Indicates Assigned Logic

Assign Instances to Region Region name: UserRegion0	×
Assignable instances: Icd_instance/count[0] Icd_instance/count[1] Icd_instance/count[2] Icd_instance/count_7_0 Icd_instance/count_7_0 Icd_instance/count_7_0 Icd_instance/count_2_0_a2 Icd_instance/count_c2_0_a2 Icd_instance/count_n0 Icd_instance/count_n0 Icd_instance/count_n0	Assigned instances: Assign >> Assign All >> Unassign</td
71 Items, 0 Selected Filter unassigned instances: Matching pattern Connected to nets matching pattern Connected to ports matching pattern	0 Items, 0 Selected Filter assigned instances: Filter Filter Show I Isage
Icd_instance*	OK Cancel Help





ChipPlanner Display Settings

- Users Can Show/Hide Object and Assign Color to Resource
 - View > Display Settings

	Properties			×
	Object Type	Visible	Color	-
1	Combinatorial Cells			
2	Sequential Cells	<u> </u>		
3	IO Sequential Cells	<u> </u>		
4	IO FIFO	<u> </u>		
5	IO Pads	<u> </u>		
6	Buffer	ম		
7	RAM	<u> </u>		
8	PLL	ম		
9	Routed signal to PLL interface	ম		
10	PLL Output West Module	•		
11	PLL Output East Module	<u> </u>		
12	Clock Chip Level Multiplexor	<u> </u>		
13	IO FIFO block control	•		
14	Cluster			
15	Super Cluster			ΞÌ
Save	 / Load Display Properties Default Load 		Save	


ChipPlanner Viewing Nets

Select Net View Options from Nets Toolbar:





View Ratsnest





ChipPlanner Highlighting Nets

- Selected Nets Can Be Highlighted to Aid Analysis
 - Select Net from Design Window Nets Tab or Search Results
 - Change Highlight Color from Toolbar or Edit Menu

ChipPlanner	

🛅 File	Edit	View	Logic	Nets	Region	Т				
	Ur	ndo		Ctrl+	Z					
<u> -</u>	Re	edo		Ctrl+	Y					
월 문	Ct.	ıt		Ctrl+X						
	Co	ру		Ctrl+	C					
	Pa	iste		Ctrl+	¥					
	Se	elect All		Ctrl+	A					
	Fir	nd		Ctrl+	F					
	Hi Ur Hi	ghlight hhighlig ghlight	ht All Color	Ctrl+B nt All Ctrl+Shift+B Color Ctrl+R						





ChipPlanner

ProASIC3/E, ProASIC3L, Fusion, IGLOO/e, Axcelerator

- Floorplanning Capabilities
 - Define Rectangular Regions
 - Empty, Exclusive and Inclusive Region Support for Axcelerator
 - Modify Region types (Inclusive / Exclusive)
 - Assign Logic and Nets to Region
 - I/O Assignments
 - PLL and RAM Assignments
 - Drag and Drop Assignments
 - Multi-region Assignments NOT Recommended

] 🖺 🕄 🥌 🗾 🕖 🙌 N N 🗰 🖉	₽	B	« • I	▶ ▶ ≤	S 5. 5	20	
<u> </u>							
ST LOCK 12 n	0111101110						
HIM CO PLL_PWRDWN_pad							
	LU						
PLL_CLKINTW_INST_5							
😟 🐨 🌍 U4_PLL_H_T		P					
PLL_CLKINTW_INST_4							
I I IIII IIII IIIIIIIIIIIIIIIIIIIIIII							
		<u> </u>					



Quadrant Clock Region Support ProASIC3/E, ProASIC3L, Fusion, IGLOO/e

- Create Quadrant Clock Regions with PDC or in ChipPlanner
 - PDC Syntax:
 - assign_quadrant_clock -net netname -quadrant quadrant_clock_region [-fixed value]
 - quadrant_clock_region is UL, UR, LL, LR





Local Clock Region Support ProASIC3/E, ProASIC3L, Fusion, IGLOO/e

- ProASIC3/E, IGLOO/e and Fusion Local Clock Regions
 - Created through PDC only
 - PDC Syntax:
 - assign_local_clock -net netname -type clock_type clock_region
 - clock_type is either chip or quadrant
 - clock_region:
 - A multi-spine rectangle defined as [T | B]#:[T | B]#
 - A single spine defined as T# (Top spine) or B# (Bottom spine)





Actel Corporation Confidential © 2009

Local Clock Region Support **Axcelerator**

- Axcelerator Local Clock Regions
 - Created through PDC only
 - PDC Syntax:
 - assign_local_clock -type routing_resource_type -net netname <local_clock_region> [local_clock_region] [local_clock_region] ...
 - routing_resource_type is either hclk or rclk
 - local_clock_region is Hierarchical Resource Name of Specific Clock Region





Hands-on Labs 5 and 6

- Complete Labs 5 and 6 in the Lab Guide
- Lab 5
 - Open Designer and Compile Design
 - Save your Work
- Lab 6
 - Use PinEditor to Make pin assignments
 - Export Pin Report



Entering Timing Constraints

Timing constraint flow





Timing Requirements / Exceptions

- Timing Requirements Are:
 - Clock Frequency
 - Input Delay
 - Output Delay
- Timing Exceptions Are:
 - Multi-cycle Paths
 - False Paths
 - Maximum Delay
 - Minimum Delay
- Timing Requirements And Exceptions:
 - Direct Synthesis Mapping
 - Guide Place and Route and Timing Analysis of a Design



Timing Constraints Clock Frequency

 Clock Constraints Define the Timing Requirements Between Flip Flops For Each Clock Network





Timing Constraints Input Delay

- Input Delay Specifies When a Signal Arrives at The Input Ports of the FPGA
 - Referenced from the Launch Edge Outside the FPGA



Timing Constraints *Output Delay*

- Output Delay Specifies When the Arrives at the Input Ports of Another Device
 - Referenced to the Capture Edge Outside the FPGA





Timing Exceptions *Multi-cycle Paths*

 Multi-cycle Paths Are Paths Where the Allowable Data Path Delay is More Than One Clock Cycle





Timing Exceptions False Paths

- False Paths are Design Paths That are Ignored for Optimization and Timing Analysis
- A Path May be False Because:
 - It Doesn't Propagate Data Forward
 - The Circuitry Involved Will Operate Slower Than The Constraints
 Indicate
 - For Example, Test Logic May Be Operated At A Lower Frequency



Synplicity SDC File

- Synplicity Generates an SDC Constraint File That can be Imported Into Designer
 - Constraint file is visible on Libero File Manager tab



Importing SDC Timing Constraints

- SDC Timing Constraints can be Imported into Designer as Source File From Libero
 - Libero Automatically Sends Timing Constraints to Designer
- Specify Constraint file from Libero Menu
 - Project > Files Organization > Designer Constraint files





SmartTime Overview

- SmartTime is Actel's Static Timing Analysis Tool for:
 - ProASIC3, ProASIC3L, Fusion, IGLOO, APA and 500K
 - SX-A, RTSX-S, eX, AX, RTAX-S
 - All Future Products



SmartTime Features

- Graphical Constraint Entry
- SDC Constraint Support
- SDC Constraint Checker
- Analysis
 - Cross-clock Domain Analysis
 - Flexibility in Clock Domain Selection
- Improved Ease-of-Use
 - Separate Constraint & Analysis Views
 - Separate Maximum & Minimum Analysis Views
 - Clock Domain Browser for the Analysis View
 - Visual Constraint Dialogs
 - Customizable Timing Information for the Paths List
 - Constraint Entry from the Analysis Window
 - Customizable Timing Reports
 - Filtering Capabilities
 - Persistence of User Settings



SmartTime Supported SDC Constraints

- Timing Requirements and Exceptions can be Entered
 - From a Synopsys Design Constraint (SDC) File or
 - The SmartTime Visual Dialog GUIs
- SDC Constraints Supported in SmartTime:
 - oreate_clock
 - oreate_generated_clock
 - set_clock_latency
 - set_input_delay
 - set_output_delay
 - set_load
 - set_false_path -from -through -to
 - set_ multicycle_path -from -through -to
 - set_ maximum_delay -from -through -to
 - set_ minimum_delay -from -through -to



SmartTime Windows

- SmartTime Includes of Separate Constraint Editor and Timing Analysis Windows
 - Constraint Editor GUI Based Constraint Entry
 - Timing Analyzer Provides Delay Information





Actel Corporation Confidential © 2009

SmartTime Constraints Editor

SmartTime [find_min *] - [Constraints Editor]	
😳 Eile Edit View Actions Iools Window Help	_ 8 ×
8 8 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	
Constraints Requirements Generated Clock Generated Clock Dutput Delay Cutput Delay Kax Delay Max Delay Multicycle False Path Advanced Clock Source Latency Disable Timing Clock Uncertainty	
Ready	Temp: COM Volt: COM Speed: -2

- Use Constraints Editor to:
 - Enter or Edit Timing Requirements:
 - Clock Frequency, Clock Latency, Input and Output Delays
 - Enter or Edit Timing Exceptions:
 - Max Delay, Multicycle Paths, False Paths
 - Browse Clock Domains
- Constraints are grouped as Requirements and Exceptions



SmartTime Toolbar

- The SmartTime Toolbar Contains Commands for Performing Common Operations.
 - Tool Tips Are Available for Each Button.





SDC Constraints in SmartTime

							1		1-		1			20
Constraints		Synta:	x Output port	s C	lock	Clk To Out Max (ns)	Clk To	Out Ma: nsì	k Delay M (ns)	lin Delay (ns)	Clock	File	C	;om
		Click he	ere to add a cons	traint)		
Generated Clock	1	٣	DataMin[0]	melk					2.500	2.500	rising	D:/Actelprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, lin	e 35	
🔨 Input Delay	2	*	DataMin[1]	melk					2.500	2.500	rising	D:/Actelprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, lin	e 36	
🕈 Output Delay														
Exceptions														
Max Delay														
Min Delay														
Multicycle													_	
🕒 Constraints Editor														
E- Constraints	— r				CI 1	Setup	Hold Ma	x Delav	Min Dela	v Clock		F 1 0		T
		5	yntax Input p	orts	LIOCK	(ns)	(ns)	(ns)	(ns)	Edge			nment	s
Clock		CI	lick here to add a	constraint										
Generated Clock		<u> </u>	STROB	in molk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 26		
		2 7	A_in[0]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 27		
Uutput Delay		3 7	A_in[1]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 28		
Exceptions		<u>4 7</u>	B_in[0]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 29		
Min Delau		5 7	B_in[1]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 30		
Millicycle		<u>3 7</u>	C_in[0]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 31		
False Path		<u>/ </u>	C_in[1]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 32		
Aduanced		3 7	D_in[0]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 33		
E Auvanceu		<u>9 (</u>	D_in[1]	mclk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 34		
Clock Source Latency		10 🛛	<pre>// mrst_n</pre>	melk				7.500	7.500	rising	D:/Acte	lprj/Bootcamp_stuff/find_min_85/synthesis/find_min_sdc.sdc, line 37		
Clock Source Latency		<u> </u>												
Clock Source Latency Disable Timing Clock Uncertainty	ŀ													

Path to constraint file



Clock Constraints

SmartTime Clock Domains

- SmartTime Detects Possible Clocks by Tracing Back from the Clock Pins of all Sequential Components Until it Finds:
 - An Input Port
 - The Output of Another Sequential Element, or
 - The Output of a PLL
- SmartTime Classifies Clock Sources Into Three Types:
 - Explicit Clocks
 - Potential Clocks
 - Clock Network
- Each Clock Domain Contains at Least 3 Path Sets:
 - Register to Register
 - External Setup or Hold
 - Clock to Out



SmartTime Constraint Entry

- Enter Timing Requirements Prior To Layout For Timing Analysis And To Guide Layout Engine
 - Clock Frequency, Input and Output Delays
- Timing Exceptions Can Be Entered After Layout If Negative Slack Exists To Ensure Correct Timing Analysis
 - Max Delay, Multicycle Paths, False Path





Entering Clock Constraints

Visual Constraint Dialog Box Simplifies Constraint Entry





SmartTime Clock Constraints

- Clock Constraints in Constraint Editor
 - Select Constraint to Add, Edit or Delete





SmartTime Generated Clock Constraints

- Constraints For Internally Generated Clock Can Be Specified Using Generated Clock Constraints
 - Useful For Constraining Designs with Clock Dividers





Entering Generated Clock Constraints

Visual Constraint Dialog Box Simplifies Constraint Entry





SmartTime Generated Clocks



S7 Constraints Editor										
🖃 Constraints		Syntax	Clock Name	Clock Pin	Reference Pin	Multiplier	Divider	Waveform	File	Comments
E Requirements		Click here	e to add a consti	raint						
Clock	1	٣	CLK100_by3	clk_div[1]:Q	clk_in	1	3	synchronized	GUI	
Generated Clock										
Input Delay										
Uutput Delay										
- May Delay										
Multicucle										
False Path										
Advanced										
Clock Source Latency										
data!										



SmartTime

Automatic Creation of Generated Clocks

- Automatic Creation of Generated Clock Constraint Based on Static Configuration of PLLs for Fusion, ProASIC3, IGLOO, AX, RTAX-S
- No Effect Unless the Reference Clock is Constrained

Constraints Editor									
🖂 Constraints		Syntax	Clock Pin	Reference Pin	Multiplier	Divider	Waveform	File	ē
🛱 🔤 Requirements	1	7	d2:Q	d2:CLK	1	2	synchronized	D:/ftc/axgc1/i1.sdc, line 2	
Clock	2	Y	plli/PLL_INT:CLK2	plli/PLL_INT:REFCLK	2	1	synchronized		1
🕂 🔨 Generated Clock	3	Y	plli/PLL_INT:CLK1	plli/PLL_INT:REFCLK	2	6	synchroni 🛛 Ə	iuto-generated	ן נ
□ Input Delay □ Coutput Delay □ Exceptions □ Max Delay □ Multicycle □ False Path □ Advanced □ Clock Source Latency	1								



Clock Source Latency: *Definition*

- Specify Delay When Clock is Generated Outside the Design
- Specify Clock Jitter



 Clock Source Latency can be Attached to any Clock Constraint (Internal or External)



Clock Source Latency: Constraint Specification

- Specify Clock Insertion Delay and Jitter
- Specify Early and Late Times for Rising and Falling Edges

• SmartTime [find_min *] - [Constr	raints E	Ita _ T Edit Evisting Clark Course Latence		
😳 File Edit View Actions Tools Wind	dow <u>H</u> el	Luit Existing Clock Source Latency		_ 8 ×
6 6 66 7 x 92		Clock Name or Source: mclk	.	🖳 🙅 💁
⊡ Constraints	S			ents
Requirements	Cli	f		
Generated Clock		Clearly Courses		
Input Delay				
Output Delay		Late Rise 0.500 ns	Late Fall ns	
		Early Rise -0.250 ns	Early Fall ns	
Max Delay				
Min Delay Multicucle				
False Path				
		Clock Name or Source		
Clock Source Latency		Clock Edges: 📃 Falling same as rising	🔲 Early same as late	
Disable Timing				
Clock Uncertainty		Comment:		
·		I		
Ready				Temp: COM Volt: COM Speed: -2
		Help	OK Cancel	



SmartTime Virtual Clocks

- A Virtual Clock has no Associated Source
 - Used to describe clocks outside the FPGA that have an impact on timing analysis inside the FPGA
- Clock Analysis for Virtual Clocks
 - Specify a constraint for a clock that is running outside the FPGA and do timing analysis on the design as it interacts with this "virtual" circuitry


Input and Output Delay Constraints

SmartTime Input Timing Constraints

- Input Timing Constraints can be Entered as Input Delay or External Setup/Hold
 - Input Delay Delay in Terms of Delay Budget Outside FPGA (Default)
 - Referenced from the Launch Edge Outside the FPGA
 - Generally Used by Synthesis Tools
 - External Setup / Hold Specify Input Delay Budget Inside FPGA
 - Referenced to the Capture Edge Inside the FPGA
 - Used by Previous Actel Timer



Input Constraints Input Delay

Visual Constraint Dialog Box Simplifies Constraint Entry



Input Delay Constraints External Setup / Hold

/ Select External Setup/Hold





Input Delay / External Setup What do These Constraints Mean?

Input Delay Period = 13.9 ns 5 ns |4ņs |10ns |12ns |18ns Oņs |2ns 6ns |8ns 14ns |16ns | |20ns | |22ns | |24ns |26ns |28ns |30ns mclk A_in mrst_n STROBEn Input delay = 5 ns; B in Input arrives 5 ns after launch edge Cin D in DataMin

External Setup

	P	eriod = 13.9 ns				
	5 ns	8.9 ns				
	0ns 2ns 4ns	6ns 8ns 10ns 12ns	14ns 16ns 18ns	20ns 22ns	24ns 26ns	28ns 30ns
mclk		F				<u></u>
A_in		×	<u>\</u>			
mrst_n						
STROBEn		External setup = 8.9 ns				
B_in		Data arrives 8.0 ps before conture edge				
C_in			e capille euge			
D_in						
DataMin						



SmartTime Output Delay Constraints

- Output Delay Defines the Delay of an Output Relative to a Clock
 - Clock-to-Output: Specifies the Output Delay Timing Budget Inside the FPGA (default)
 - Referenced from the Launch Edge Inside the Current Design
 - Output Delay: Specifies Output Delay Timing Budget Outside the FPGA
 - Referenced to the Capture Edge Outside the Current Design
 - Used by Synthesis tools



Output Constraints Clock-to-Output



Clock-to-Output is the Default



Output Delay Constraints Output Delay





Clock to Output / Output Delay What do These Constraints Mean?



Output Delay





Timing Exceptions

Timing Exceptions False Paths

- The False Path Constraint Removes Timing Requirements on Specified Paths
 - Starting Points Are Input Ports or Register Clock Pins
 - Ending Points Are the Register Data Pins or Output Ports
- False Paths Are Not Considered During the Timing Analysis
- False Path Constraints Take Precedence Over Multiple Cycle Path Constraints and Overrides Maximum Delay Constraints



SmartTime Entering False Path Constraints

Specify From, To, Through Pins





False Path Constraint Source Pins

Specify Starting Point for False Path

Select Sou	rce Pins for	False Path Cor	nstraint 🛛 🔀
Specify pins	• by explicit list	C by <u>k</u> eyword and w	ildcard
Available Pins:			Assigned Pins:
CLK D0 D1		<u>A</u> dd >	
D2 FF0\$112:CLK FF1\$111:CLK		A <u>d</u> d All >	
FF3\$116:CLK FF3\$116:CLK FF4\$117:CLK RST		< <u>R</u> emove	
		< Re <u>m</u> ove All	
, Filter available	pins:		Add or remove pins
Pin Type:	All pins	▼	Trom source list
*		<u>F</u> ilter	
			ritter pin names
Help			OK Cancel



False Path Example

- Multiplexer S Input Selects Test / Normal Modes
 - Paths through MX0:A are False Paths





False Paths in Constraint Editor

False Path Constraint in Constraint Editor

• Select Constraint to Add, Edit or Delete

SmartTime [FALSE_PATHS *] - [Constraints Editor]						
💱 Eile Edit View Actions Tools	<u>W</u> indow <u>H</u> elp					- 🖻 ×
o 🗿 🖻 🖬 🗹 🗅	2 🔀	®≍ 2	🕑 📶 🐜 🍒	■ <mark>≫ > > </mark> ?	5 S	
🖃 Constraints	Syntax	From	Through	To	File Comments	
🚊 Requirements	Click here to ac	ld a constraint				
Clock	1 🚩		[get_pins { MX0:A }]		GUI	
Generated Clock				·	· · · · · · · · · · · · · · · · · · ·	
Input Delay						
Output Delay						
Max Delay						
Min Delay						
Multicycle						
False Path						
🖻 Advanced						
Clock Source Latency						
, Ready	, ,				Temp: COM Volt:	COM Speed: -F



Timing Exceptions *Multicycle Paths*

- The Multicycle Path Constraint Overrides the Single Cycle Timing Requirement Between Sequential Elements
 - The Number of Clock Cycles for Setup or Hold Check Is Specified in the Constraint
- False Path Constraints Take Precedence Over Multicycle Path Constraints





SmartTime

Entering Multicycle Path Constraints

- Specify Path Multiplier and From, To, Through Pins
- Add Path Multiplier



Set Multicycle Constraint



×

Timing Exceptions Maximum Delay

- The Max Delay Constraint is Used to Specify The Maximum Delay for Timing Paths in The Design
- Max Delay is a Timing Exception and Overrides The Timing Requirement Between Flip Flops
 - Maximum Delay Involving Registers Takes Clock Insertion and Setup/Hold Delays Into Account
- Max Delay Can Also be Used to Constrain Combinatorial Input to Output Paths



Timing Exceptions Maximum Delay

- Specify Maximum Delay Constraint
 - Overrides Clock Constraint





Timing Exceptions *Minimum Delay*

- Specify Minimum Delay Constraint
 - Overrides Clock Constraint





SmartTime Constraint Wizard

SmartTime Constraints Wizard

- Step by Step Guidance to Create Timing Constraints
 - Overall Clock
 - Overall I/O
 - Specific Clocks
 - Generated Clocks
 - Specific Inputs
 - Specific Outputs
- Summary
 Displays all
 Constraints
 Entered

Constraint Wizard Constrain You can set	ing explicit clocks a constraint for all explicit clocks in your design.
Specific input constraints Specific output constraints Summary Help	The constraint above will apply to all explicit clocks that are not constrained yet. You will be able to override this constraint for any specific clock in a later step of this Wizard.

Opening the Constraint Wizard: Tools > Constraint Wizard



SmartTime Constraints Wizard





Exporting SDC Timing Constraints

 Constraints Entered in SmartTime GUI Can Be Exported from Designer





Constraint Recommendations

- Set Realistic Constraints
- Set Sufficient Constraints
- Don't Over constrain
 - Improperly-Constrained Design Can Lead to Long Run Times, Multiple Iterations and/or Sub-optimal Results
- Enter any Known Exceptions
 - Exceptions can be Added During Timing Analysis



Designer Layout Options

Layout

- Assign Physical Locations to Unassigned I/Os
- Place Logic Modules
- Assign Routing Tracks to Nets
- Calculate Detailed Delays for All Paths



Layout Options ProASIC3, ProASIC3L, Fusion, IGLOO

Layout Options	
✓ Timing-driven	
Power-driven	
🔽 Run <u>p</u> lace	
Place incrementally	
🔲 Lock existing placement	
🔽 Run <u>r</u> oute	Multi-Pass Configuration
Route incrementally	Number of passes: 5
	1 25
Use <u>M</u> ultiple Passes	Start at seed index (1 - 101):
Configure	
	Measurement: Slowest clock
Ad <u>v</u> anced	C Specific clock
	C Iming violations
<u>H</u> elp C	🕫 Ma <u>x</u> imum delay 🛛 C. Minimum <u>d</u> elay
	Select <u>by</u> ; Worst Slack
	Stop on first pass without violations
	C Total power
	Sa <u>v</u> e design file for each pass
	Help OK Cancel

- Layout Mode
 - Timing-Driven: Constraints Defined in SmartTime
 - Power-Driver: Reduces Power Consumption
- Incremental Placement and Routing
- Multi Pass Layout Option
 - P&R Runs Multiple Times
 - Specify:
 - Number of Iterations
 - What to Optimize (Specific Clock, Timing Violations, Total Power)
 - Which Results to Save (Best or All)
- Advanced Layout Options
- Known Limitations
 - Router Cannot Run in Incremental Mode if there Has Been Change in Global Assignments
 - Users Must Manually Uncheck Incremental Routing Option and Re-run Layout



Advanced Layout Options ProASIC3 ProASIC3L, Fusion, IGLOO

Layout Options		
✓ Timing-driven ✓ Power-driven		
 Run glace Place incrementally Lock existing place Run route Route ingrementa Use Multiple Passes Configure 	acement (Eix) Ily	
	Advanced Layout Options	
Ad <u>v</u> anced		Restore <u>D</u> efaul
Help	Timing-Driven Figh effort layout Enables the physical synthesis of combinat	ional logic.
	J Sequential optimization Enables the physical synthesis of sequences of sequenc	ential logic.
	Router: Repair minimum delay violations The router attempts to repair paths that delay violations or hold time violations.	have minimum
	<u>Н</u> ер ОК	Cancel

- High Effort Layout Mode
 - Placer uses additional netlist optimizations to improve performance (up to 10% QOR increase)
 - Layout runtime will increase (average 2x)
 - Can combine this option with the Multi-Pass mode to achieve the best possible performance
- Repair Minimum Delay Violations
 - An additional route is performed that attempts to repair paths that have minimum delay and hold time violations
 - Done by increasing the length of routing paths and inserting routing buffers to add delay to paths
 - No additional tiles or modules are inserted
 - The amount of delay inserted is limited
 - Best suited to repair paths with small (0 to 3 ns) hold and minimum delay violations



Sequential Optimization

- Power-driven + High-effort + Sequential optimization
 - 8.4
 - No-op
 - Otherwise, SEQ tiles increase by 6.5% on average
 - High-effort itself reduces COMB tiles by 6.1% on average
 - 8.4_SP1
 - Remove duplicate registers that are driven by the same net
 - SEQ tiles reduce by 3.3% on average
 - 8.5_SP1
 - Perform forward retiming of registers towards output I/Os



Designer Power-driven Layout ProASIC3, Fusion, IGLOO, Axcelerator

- Layout Optimization Reduces Power Consumption
 - Reduces net capacitance based on estimated activities
 - Re-places instances and Optimizes Clock Tree distribution
 - Average ~18% reduction in *<u>net power</u>*
 - Up to 50% in some designs. Includes clocks and regular nets
 - Average ~13% reduction in <u>total power</u>
 - Up to 33% in some designs. IGLOO designs with 5pf output load and LVCMOS 1.5V I/Os
 - Little to no effect on timing performance
 - Typically less than -2%







Quadrant Clock Assignment ProASIC3, Fusion, IGLOO

- Finds And Creates Legal Clock Assignments for Clock nets not Already Assigned by the User
- Runs Automatically As Part Of Layout
- Performs Auto-assignment of nets Given Certain Criteria
 - Runs when > 6 globals (or > 2 PLLs are detected)
 - Globals come from user netlist or PDC constraints
 - CCC macro instantiation
 - Global promotion through PDC constraints
 - If > 6 global nets, LCA will assign the global nets to
 - Chip wide globals or
 - Quadrant regions
 - The choice of chip wide globals or a quadrant region will depend on
 - Fanout of the nets
 - Resources and user constraints
 - Shared loads



Layout Options ProASIC^{PLUS}

Layout Options	
Timing- <u>d</u> riven	
 Run glace Place incrementally Lock existing plane Run route Route incremental 	icement (<u>Fi</u> x) Il y
✓ Use <u>M</u> ultiple Passes	Multi-Pass Configuration
Configure	Maximum number of passes: 5
<u>H</u> elp	Meas <u>u</u> rement:
	Save results from all passes
	Help OK Cancel

- Layout Mode
 - Timing-Driven: Constraints Defined in SmartTime
 - De-selecting Causes Standard Layout to be Used
- Place and Route Tools
 - Can Be Turned On or Off
- Incremental Placement and Routing
 - Lock Existing Placement: Treats All Unchanged Macros as Fixed Placements
- Multi Pass Layout Option



Layout Options Axcelerator

Layout Options	X	
✓ Timina-driveni ✓ Power-driven		
🔽 Run glace		
Place incrementally		
🔲 Lock existing pla	acement (Eix)	
<u>E</u> ffort level: 3		
<u></u>		
Low	High	
✓ Run <u>r</u> oute ✓ Route in <u>c</u> rementally	,	
Use <u>M</u> ultiple Passes		
Configure	Advanced Layout Options	
		Restore <u>D</u> efau
Ad <u>v</u> anced	Timing-driven Router	
Help	I he router attempts to repair paths that delay violations or hold time violations.	have minimum
	Help OK	Cance

Layout Mode

- Timing-Driven
 - Constraints Defined in SmartTime
 - De-selecting Causes Standard Layout to Be Used
 - Power Driven
- Incremental Placement and Routing
 - Lock Existing Placement: Treats All Unchanged Macros as Fixed Placements
- Placement Effort Level
 - Provides Degree of Control over Timing-Driven Placement Engine
- Range is from "Low" to "High"
- Multi Pass Layout Option
- Repair Minimum Delay Violations



Layout Modes SX Architecture

Layout Options	×
Timing- <u>D</u> riven	ОК
Place Incrementally	Cancel
Lock Existing Placement (<u>Fix</u>)	Help
Use <u>M</u> ultiple Passes	
Configure	
Ad <u>v</u> anced	

Advanced Layout Options	×
Extended <u>Run</u>	ОК
Timing-Driven-	Cancel
Effort Level	
I00 ₽	<u>H</u> elp
Restore <u>D</u> efaults	

Layout Mode

- Timing-Driven: Constraints Defined in SmartTime (SX-A) or Timer (SX)
 - De-selecting Timing-Driven Layout Selects Standard Layout
- Incremental Placement
 - Lock Existing Placement: Treats All Unchanged Macros as Fixed Placements
 - De-selecting Allows Placer to Relocate Unchanged Macros if Necessary
- Multiple Passes
 - P&R Runs Multiple Times
- Advanced Options Allow Additional Control of Timing-driven Placement Engine
 - SX, SXA and eX Families



Which Layout Mode to Use?




Completed Layout





Designer Files and Reports

Exporting Files

Supported File Types (File>Export)

Files	File Extension	Export Type	Family
Actel Flattened Netlist	*.afl	Netlist file	All
Actel Internal Netlist	*.adl	Netlist file	All
Standard Delay Format	*.sdf	Timing file	All
STAMP	*.mod, *.data	Timing file	SX-A, eX, Axcelerator, IGLOO/e, ProASIC3/E, Fusion, ProASIC, ProASIC PLUS
Tcl script file	*.tcl	Script file	All
Verilog Netlist	*.v	Netlist file	All
VHDL Netlist	*.vhd	Netlist file	All
EDIF Netlist file	*.edn	Netlist file	All
Log File	*.log	Log file	All
STAPL	*.stp	Programming file	Fusion, IGLOO/e, ProASIC3/E, ProASIC, ProASIC <u>PLUS</u>
Bitstream	*.bit	Programming file	Fusion, IGLOO/e, ProASIC3/E, ProASIC, ProASIC <u>PLUS</u>
Programming file (legacy)	*.fus	Programming file	ACT1, ACT2, ACT3, MX, 1200XL, 3200DX
Actel programming file	*.afm	Programming file	ACT1, ACT2, ACT3, MX, 1200XL, 3200DX, SX, SX-A, eX, Axcelerator
Location constraint file	*.loc	Other file	SX-A
Routing Segmentation file	*.seg	Other file	Axcelerator, IGLOO/e, ProASIC3/E, Fusion, ProASIC, ProASIC PLUS
Silicon Explorer Probe file	*.prb	Debugging file	ACT1, ACT2, ACT3, MX, 1200XL, 3200DX, SX, SX-A, eX, Axcelerator



Exporting Files - Cont.

Files	File Extension	Export Type	Family
ProASIC Constraints file	*.gcf	Constraints file	ProASIC
ProASIC <u>PLUS</u> Constraints file	*.gcf	Constraints file	ProASIC ^{PLUS} (Timing constraints in GCF are not supported)
Combiner Info	*.cob	Other file	ACT1, ACT2, ACT3, MX, 1200XL, 3200DX, SX, SX-A, eX, Axcelerator, IGLOO/e, ProASIC3/E
BSDL file	*.bsd	Debugging file	3200DX, MX, SX, SX-A, eX, Axcelerator, Fusion, IGLOO/e, ProASIC3/E, ProASIC, ProASIC ^{PLUS}
Criticality	*.crt	Constraints file	ACT1, ACT2, ACT3, MX, 1200XL, 3200DX
I/O buffer information specification (IBIS)	*.ibs	Other file	MX, ProASIC ^{PLUS} , IGLOO/e, ProASIC/E; the IBIS file provides a standard file format for recording parameters like driver output impedance, rise/fall time, and input loading, which may then be used by any software application.
PIN	*.pin	Constraints file	ACT1, ACT2, ACT3, MX, 1200XL, 3200DX, SX, SX-A, eX
SDC	*.sdc	Constraints file	SX-A, eX, Axcelerator, ProASIC ^{PLUS} , IGLOO/e, ProASIC3/E, Fusion
Physical Design Constraint	*.pdc	Constraints file	Fusion, IGLOO/e, ProASIC3/E, Axcelerator
Design Constraint file file	*.dcf	Constraints file file	ACT1, ACT2, ACT3, MX, 1200XL, 3200DX, SX, SX-A, eX



Exporting Pin Report

Pin Report Can be Exported from Designer





Exporting Pin Constraint File

Pin Constraint File Can be Exported from Designer





Exporting IBIS File





IBIS File

Wtest1.ibs - HyperLynx V File Edit View IBIS Help	visual IBIS Editor	Package	choice	based o	on the	e desian
🗋 🚅 🔚 🗠 🗠 🐰						a congri
	 [Component] [Manufacturer] [Package] variable Un-comment th	RTSXS Actel Corporation typ e appropriate packs	**************************************		********* max	****
Component] RTSX5 Component	R_pkg L_pkg C_pkg	2.0 10.0nH 6.0pF	NA NA NA	ת ה ה	NA C NA C NA C)QFP208)QFP208)QFP208
End]	R_pkg L_pkg C_pkg	2.0 10.0nH 6.0pF	NA NA NA		NA NA NA	CQFP256 CQFP256 CQFP256
	R_pkg L_pkg C_pkg 	0.753 4.170nH 2.419pF	NA NA NA		NA NA NA	CCLG256 CCLG256 CCLG256
	 Note: TTL5V - 5V TT CE055V - 5V C LVTTL - 3.3V PC13V - 3.3V PC13V - 3.3V PC15V - 5.0V HS - High LS - Low 2	L standard MOS standard TTL standard PCI standard PCI standard Slew lew				
	[Pin] signal_r 2 abus[1] 3 abus[2] 4 abus[3] 5 xbus[10] 6 xbus[11] 7 xbus[12] 8 xbus[13] 9 clk_y	ame model_ CMOS5V_I CMOS5V_I CMOS5V_I PCI5V PCI5V PCI5V TTL_5V_F	_name .S .S .S	R_pin	L_pin	C_pin
	W		i			
Cust	omized Pl model nam	N list with ones and sig	corresp nal nai	oonding mes		

More on IBIS later in the week . . .



Post-Layout Timing Analysis

Timing Analysis

- Timing Terminology
- Timing Analysis with SmartTime
- SmartTime Timing Reports
- Reference



Timing Terminology

Timing Terminology: Arrival Time

- Arrival Time is the Sum of:
 - The Clock Network Delay to the Source Flip-Flop
 - The Delay from the Source Flip-Flop to the Destination Flip-Flop





Timing Terminology: *Required Time*

- Required Time is:
 - Clock Period Plus Clock Network Delay to Destination Flip-Flop
 - Minus the Setup Requirement for the Destination Flip-Flop





Timing Terminology: Slack

- Slack =
 - Required Time Arrival Time (setup check)
 - Arrival Time Required Time (hold check)
 - Violation of Slack < 0



Timing Analysis with SmartTime

Timing Analysis with SmartTime

- Design Summary
- Maximum Delay Analysis View
- Minimum Delay Analysis View
- Cross Clock Domain Analysis
- Removal and Recovery Checks
- SmartTime Scenarios



SmartTime Analysis View Design Summary

- Performance Summary is Displayed in Maximum and Minimum Delay Analysis View
 - $\sqrt{-1}$ Indicates Timing Requirements Met for That Domain
 - X Indicates There Are Violations Within the Domain





Timing Analysis with SmartTime

Design Summary

- Maximum Delay Analysis View
- Minimum Delay Analysis View
- Cross Clock Domain Analysis
- Removal and Recovery Checks
- SmartTime Scenarios



Maximum Delay Analysis View Register to Register Path Set

Identify Internal Setup Violations





Maximum Delay Analysis View Register to Register Path Set (cont.)

- Verify Internal Timing Requirements and Identify Paths With Violations
- By Default The Register to Register Path Displays:
 - Source Pin And Sink Pin Beginning And Ending Points For Delay Calculation
 - Delay Path Delay From The Clock Pin Of The Source Flip-flop To The Input Of The Destination Flip-flop
 - Slack Required Time Arrival Time
 - Arrival Delay From The Launch Edge At The Source Flip-flop To The Data Input Of The Destination Flip-flop
 - Required Time Data Must Be Valid To Avoid A Timing Violation; Calculated From Clock Period And Setup Requirement For Destination Flip-flop
 - Setup Setup Time Requirement For The Destination Flip-flop
 - Minimum Period Minimum Clock Period To Avoid A Timing Violation
 - Skew Clock Insertion Delay To The Source Flip-flop Minus The Clock Insertion Delay To The Destination Flip-flop
- Timing Information For Each Type Of Set Can Be Customized



SmartTime Internal Setup Check

Setup Check is Displayed in Maximum Delay Analysis
 View in Register to Register path set



Setup Check Calculation

- Arrival time = Launch edge (0) + max Clock to FF1 + max Data path
- Required time = Capture edge (T) + min Clock to FF2 Setup of FF2
- Slack = Required Arrival = Violation if < 0



Setup Check in SmartTime

n Delay Analysis	View										
	From	*			To	*	8				
							Apply Filter	Store	Filter	Reset Filter	
ary clk2		Source P	in	Sink Pin	D	elay ns)	Slack	Arrival (ns)	Required (ns)	Setup (ns)	Ī
Cik i Register to Register	1	reg1/U0:CLK	reg3/U	0:D		1.475	8.291	4.523	12.814	0.234	-
xtemal Setup			in passed and	000044121		Nation of Contract		100000000		-N	
k to Output	<				111						
Pin		Pin Name	Type	Net Name	Cell Name	0p	Delay (ns) Total (ns	s) Fanout E	dae	
Output	1	From: reg1/U0:C	K			_					l
r Sets	2	To: rea3/U0:D									L
	3	data required time						12.81	4		l
	4	data arrival time				-		4.52	23		l
	5	slack						8.29	1		l
	6							1.0000			1
		Data arrival time	calculation								l
	7	clk1			-		0.000	0.00	0		l
	8	reg1/U0:CLK	clock network			+	3.048	3 3.04	18 r		
	9	reg1/U0:Q	cell		ADLIB:DFEG	+	0.673	3 3.72	21 1 r		
	10	a2_1:A	net	s3		+	0.106	3.82	27 r		
	11	a2_1:Y	cell		ADLIB:AND2	+	0.641	4.46	68 2 r		
	12	reg3/U0:D	net	s5		+	0.055	5 4.52	23 r		
	13	data arrival time						4.52	23		ſ
	14										i.
		Data required tir	ne calculation							15	
	15	clk1	Clock Constraint				10.000	10.00	00		
	16	reg3/U0:CLK	clock network			+	3.048	3 13.04	18 r		
	17	reg3/U0:D	Library setup		ADLIB:DFEG	-	0.234	4 12.81	4		
	18	data required time					1	12.81	4		

Setup

- Arrival time = Launch edge (0) + max Clock to FF1 + max Data path
- Required time = Capture edge (T) + min Clock to FF2 Setup of FF2
- Slack = Required Arrival = Violation if < 0



Clock Source Latency: Analysis

Pin Name	Туре	Net Name	Cell Name	Ор	Delay (ns)	Total (ns)	Fanout	Edge	
From: irci:CLK									
To: iry1:D									
data required time						6.566			
data arrival time				-		8.285			
slack						-1.719			
Data arrival time calcula	tion								
clk					0.000	0.000			Late
	Clock source laten	су		+	0.500	0.500		r	
Irci:CLK	Clock network			+	5.573	6.073		r	Launch
irci:Q	cell		ADLIB:DFEG	+	0.673	6.746	1	r	
iadd2/add0_FCINST1:A	net	rci		+	0.151	6.897		r	
iadd2/add0_FCINST1:FCO	cell		ADLIB:FCINIT_BUFF	+	0.543	7.440	1	r	
iadd2/add0:FCI	net	iadd2/add0_FCNET1		+	0.000	7.440		r	
iadd2/add0:FCO	cell		ADLIB:ADD1	+	0.075	7.515	1	r	
iadd2/add1:FCI	net	iadd2/c0		+	0.000	7.515		r	
iadd2/add1:S	cell		ADLIB:ADD1	+	0.610	8.125	1	r	
iry1:D	net	sy[1]		+	0.160	8.285		r	
data arrival time						8.285			
Data required time calcu	lation								
clk	Clock Constraint				4 000	4 000			Early
	Clock source laten	су		+	-0.250	3.750		r	Lairy
iry1:CLK	Clock network			+	3.050	6.800		r	Cantur
iry1:D	Library setup time		ADLIB:DFEG	-	0.234	6.566			Jupiu
data required time						6.566			



Setup Check w/ Multicycle Path

SmartTime Uses Multicycle Path Constraint in Setup Check



- Setup Check Calculation
 - Arrival time = Launch edge (0) + max Clock to FF1 + max Data path
 - Required time = Capture edge (2T) + min Clock to FF2 Setup of FF2
 - Slack = Required Arrival = Violation if < 0



Setup Check w/ Multicycle Path

ysis viev	Ŵ.				_			-
Fr	om *			To *				
_					Apply Fi	ilter Sta	ore Filter	Reset Filte
	Source	Pin	Sink Pin	Delay (ns)	▲ Sla (n	ck Arrival s) (ns)	Required (ns)	Setup (ns)
ster 1	reg1/U0:CLK	reg3/U0:D	š	1.475	18.2	91 4.523	3 22.814	0.23
								1
<u></u>			IIII					
	Pin Name	Туре	Net Name	Cell Name	Op	Delay (ns)	Total (ns) Far	nout Edg
1	From: reg1/U0:	CLK				1.1	a data dalah	
2	To: reg3/U0:D							
3	data required tim	e					22.814	
4	data arrival time				5		4.523	
5	slack						18.291	-
6								
11	Data arrival tim	e calculation	-	-				
7	clk1					0.000	0.000	
8	reg1/U0:CLK	clock network			+	3.048	3.048	r
9	reg1/U0:Q	cell	-	ADLIB:DFEG	+	0.673	3.721	1 r
10	a2_1:A	net	s3		+	0.106	3.827	r
11	a2_1:Y	cell		ADLIB:AND2	+	0.641	4.468	2 r
12	reg3/U0:D	net	s5		+	0.055	4.523	r
13	data arrival time						4.523	
14	-							
	Data required	ime calculation						
15	clk1	Multicyle Constraint				20.000	20.000	
16	reg3/U0:CLK	CIOCK HELWOIK			+	3.048	23.048	r
17	reg3/U0:D	Library setup		ADLIB:DFEG	-	0.234	22.814	
18	data required tim	e					22.814	

Setup Check

- Arrival time = Launch edge (0) + max Clock to FF1 + max Data path
- Required time = Capture edge (2T) + min Clock to FF2 Setup of FF2
- Slack = Required Arrival = Violation if < 0</p>



SmartTime External Setup Check

- External Setup Defines the Timing Requirements at the Input Pins
- External Setup Check is Displayed in the Maximum Delay Analysis View for Each Clock Domain







SmartTime External Setup Check No Input Constraints

≽ Maximum Delay Analysis Vi	iew											
	From	*				To *						_
MAX												
in v @ clock 40 ▲							A	pply Fil	ter	Store Filter	Reset F	ilter
Register to Register		1			Belay	Slack	Arriual	Der	horium	Setun	Evternal	
External Setup		Source Pin	Sink	Pin	(ns)	(ns)	(ns)		(ns)	(ns)	Setup (ns)	
Clock to Odiput	1	cp3_in(4)	g2_4_l2/l1/bufi	n[0]:D	2.576		2.57	6		0.402	1.062	
Register to Register	2	cp3_in(1)	g2_1_l2/l1/bufi	n[0]:D	1.904		1.90	4		0.402	0.402	~
External Setup		Pin Name	Туре	Net N	ame	Cell	Name	Op	Delay (na	s) Total (ns	s) Fanout E	dge
Clock to Output	1	From: cp3_in(4)										
ie v 💮 clock_20	2	To: g2_4_l2/l1/bufin[0]:D										
Register to Register	3	data required time								NA	C	
External Setup	4	data arrival time						-		2.57	6	
Clock to Output	5	slack								NA	C	
⊡~@ g2_0_l2/l1/sclock_	6											_
Register to Register		Data arrival time calcula	tion									
External Setup	7	cp3_in(4)							0.00	0.00	0 r	
Clock to Output	8	cp3_in_pad[4]/U0/U0:PAD	net	cp3_in[4]				+	0.00	0.00	0 r	
@ g2_1_l2/l1/sclock_	9	_cp3_in_pad[4]/U0/U0:Y	cell			ADLIB:IC	PAD_IN	+	0.74	7 0.74	7 1 r	
Register to Register	10	cp3_in_pad[4]/U0/U1:YIN	net	cp3_in_pad[4	IJUO/NET1			+	0.00	0 0.74	7 r	
External Setup	11	cp3_in_pad[4]/U0/U1:Y	cell			ADLIB:IC	IN_IB	+	0.03	2 0.77	9 1 r	
Clock to Output	12	g2_4_l2/l1/bufin[0]:D	net	cp3_in_c[4]				+	1.79	7 2.57	6 r	
	13	data arrival time								2.57	6	
Register to Register	14											
External Setup		Data required time calc	ulation									
Clock to Output	15	clock_160							N/	C NA	c 🔤	
@ g2_3_l2/l1/sclock	16	g2_4_l2/l1/bufin[0]:CLK	clock network					+	1.91	6 NA	C r	
	17	g2_4_l2/l1/bufin[0]:D	Library setup			ADLIB:D	FN1C0	-	0.40	2 NA	c	

External Setup Check

- Arrival time = max Input Pad to FF
- Required time = Capture edge (T) + min Clock to FF Setup of FF
- External Setup = Arrival Required



SmartTime External Setup Check Using Input Delay Constraint

- Enter Constraint as Input Delay
 - Delay is referenced to *launch* edge of clock





SmartTime External Setup Check Using Input Delay Constraint

File Edit View Actions Iools Window File Edit View Actions Iools Window From Actions From From From	Help	Sink Pin DataDIZ1:D Type	Delay Stat (ns) (ns) 3 573 Net Name	M Image: Second system Arrival (ns) 0 257 11 073 Cell Name Image: Second system Image: Second system	Apply Require (ns) 117 Op 1	Filter S d Setup (ns) 330 0 402 Delay (ns) To	tore Filter Externa Setup (i 2 2 2 2 2 2 2 2 2 2 2 2 2	Reset Filte
Summary Solution Construction Constructi	Source Pin in(7) Pin Hame om: 0_in(7) co: DataD[7]:D ta required time ta arrival time arrival time	Sink Pin DataDIZI:D Type	Delay Slad (ns) (ns) (ns) (ns) (ns) (ns) (ns) (ns)	Image: Second system Arrival (ns) 0 257 11 073 Cell Hame 1	Apply Require (ns) 11. Op 1	Filter S d Setup (ns) 330 0 402 Delay (ns) To	tore Filter Externi Setup (i 2 otal (ns) Fa 11.330 11.073 0.201	Reset Filte
From Summary S Datasheet Max Register to Register External Setup Clock to Output To Input to Output To Datasheet External Setup User Sets	* Source Pin in[7] Pin Name om: D_in[7] DataD[7]:D ta required time ta arrival time source	DataDI71:D Type	Delay Slac (ns) (ns 3 573 Net Name	To *	Apply Require (ns) 11.2 Op 1	Filter S d Setup (ns) 330 0.402 Delay (ns) To	tore Filter Extern. Setup (r 2 otal (ns) Fi 11.330 11.073	Reset Filte
MAX Statemary Statem	Source Pin in(7) Pin Hame om: D_in(7) o: DataD[7]:D ita required time ita arrival time according	Sink Pin DataDI71:D Type	Delay Slad (ns) (ns 3 573 Hiet Name	Arrival (ns) Arrival (ns) 0.257 11.073 Cell Hame	Apply Require (ns) 11.1 Op 1	Filter S d Setup (ns) 330 0 402 Delay (ns) To	tore Filter Extern. Setup (i 2 btal (ns) Fi 11.330 11.073 0.201	Reset Filte
St Summary St Datasheet → Conck → Register to Register → Clock to Output → Clock to Output → Pin to Pin → Input to Output → User Sets	Source Pin in(7) Pin Hame om: D_in(7) o: DataD[7]:D ta required time ta arrival time and	Sink Pin DataDIZED Type	Delay Slaw (ns) (ns) 3 573 Net Name	Arrival (ns) Arrival (ns) 0.257 11.073 Cell Name	Apply Require (ns) 11: Op 1 -	Filter S d Setup (ns) 330 0 402 Delay (ns) To	tore Filter Externa Setup (r 2 otal (ns) Fa 11.330 11.073 0.201	Reset Filte
Datasheet Monometric Register Kernal Setup Clock to Output Input to Output Input to Output Stars	Source Pin in(7) Pin Hame om: D_in(7) :: DataD(7):D ta required time ta arrival time soc	Sink Pin DataD(71D Type	Delay (ns) Slat (ns) 3 573 Het Name	Arrival (ns) Arrival (ns) 0.257 11.073 Cell Name	Require (ns) 11 (0p	d Setup (ns) 330 0.402 Delay (ns) To	Extern: Setup (r 2 btal (ns) Fa 11.330 11.073	al ns) 2243 anout Edge
Kurnal Setup Clock to Output Clock to Output Input to Output Style Sets	Source Pin in[7] Pin Hame om: D_in[7] :: Data[7]:D ita required time ita arrival time source ta arrival time calcu	Sink Pin DataDI71:D Type	I let llame	Cell Name	(ns) 11: 0p	(ns) (ns) 330 0 402 Delay (ns) To	Setup (i 2 otal (ns) 11.330 11.073	ns) 2243 anout Edge
Skienal Setup Clock to Output Input to Output Input to Output Stars	Pin Hame om: D_in[7] :: Data0[7]:D ita required time ita arrival time sources	DataDI7I:D Type	Ilet Hame	Cell Name	11 : Op -	330 0.402 Delay (ns) To	2 otal (ns) Fa 11.330 11.073 0.201	2 243 anout Edge
Clock to Output Clock to Output Dutput Fri Input to Output Cost Cost Cost Cost Cost Cost Cost Cos	Pin Hame om: D_in[7] o: Data0[7]:D ta required time ta arrival time acts	Type Idation	liet liame	Cell Name	Ор -	Delay (ns) To	11.330 11.073	anout Edge
X Pin to Pin Input to Output To State	om: D_in[7] b: DataD[7]:D ita required time ita arrival time on ata arrival time calcu	lation					11.330 11.073	
Linput to Output dat dat dat dat dat dat dat dat dat da	b: DataD[7]:D ata required time ata arrival time ata arrival time calcu	lation			-		11.330 11.073 0.201	
Loser Sets dat	ata required time ata arrival time ata arrival time calcu	lation			-		11.330 11.073 0.201	
	ata arrival time ana ata arrival time calcu	lation			-		0.201	
	aon nta arrival time calcu	lation				İ	0.201	
	ata arrival time calcu	lation						
	ata arrival time calcu	lation						
			-					
	5 IX					0.000	0.000	
		Ioput Delay Constraint			+	7 500	7.600	
D	_in_pad[7]/U0/U0:PAD	net	D_in[7]		+	0.000	7.500	r
P	_in_pad[7]/U0/U0:Y	cell		ADLIB:IOPAD_IN	+	0.898	8.398	1 r
<mark>P</mark>	_in_pad[7]/U0/U1:YIN	net	D_in_pad[7]/U0/NET1		+	0.000	8.398	r
<u>P</u>	_in_pad[7]/U0/U1:Y	cell		ADLIB:IOIN_IB	+	0.032	8.430	1 r
Da	ataD[7]:D	net	D_in_c[7]		+	2.643	11.073	r
	te errivel time						11.073	
Da	ata required time ca	lculation						
mo	olk	Clock Constraint				10.000	10.000	
ma	clk_pad/U0/U0:PAD	net	molk	1	+	0.000	10.000	r
ma	clk_pad/U0/U0:Y	cell		ADLIB:IOPAD_IN	+	0.898	10.898	1 r
ma	 clk_pad/U0/U1:A	net	mclk_pad/U0/NET1		+	0.000	10.898	r
ma	 clk_pad/U0/U1:Y	cell	_	ADLIB:CLKIO	+	0.260	11.158	200 r
Da	ataD[7]:CLK	net	mclk c		+	0.574	11.732	r
Da	ataD[7]:D	Library setup time		ADLIB:DFN1C0	-	0.402	11.330	
da	ta required time	,					11.330	

External Setup Check Calculation

- Arrival time = Input Delay Constraint + max input delay to FF
- Required time = Capture edge (T) + min Clock to FF Setup of FF
- Slack = Required Arrival = Violation if < 0



SmartTime External Setup Check Using External Setup Constraint

- Enter Constraint as External Setup/Hold
 - Delay is referenced to *capture* edge of clock





External Setup Check w/ External Setup Constraint

	<u>vv</u> n k	now Geih										
	<u> 2 2</u>	i 🔰 🖉 🗖	🛛 🔁 🕅 🐜	i 🗱 🎽	a 🔊	× 3	t 🕒 🔊					
\frown		. *					т. *					
	Fron	n j.					10					
MAX										1		
P. C.									Apply Filter	Store Fil	ter Re	eset Filter
GI Summary												
		Source Pin	Sink Pin		Delay	Slack	Arrival	Requir	ed Setup	External	I	
× Begister to Begister		500100110	3000		(ns)	(ns) ´	(ns)	(ns)	(ns)	Setup (n:	s)	-
External Setup	1	_D_in[7]	DataD[7]:D		3.573	0.25	57 3.573	3	.830 0.4	02 2.:	243	
 Clock to Output 		Pin Name	Type	1 14	et Name		Cell Name	1 Op	Delay (ns)	Total (ns) Fa	anouti Eda	ell
🖃 🛼 Pin to Pin		From: D_in[7]										-
Input to Output	⊢ ⊢	To: DataD[7]:D										
🗔 🏹 User Sets		data required time								3.830		
		data arrival time						-		3.573		
		slack								0.257		
		Data arrival time calcu	ulation									
		D_in[7]							0.000	0.000	r	
		D_in_pad[7]/U0/U0:PAD	net	D_in[7]				+	0.000	0.000	r	
		D_in_pad[7]/U0/U0:Y	cell				ADLIB:IOPAD_I	V +	0.898	0.898	1 r	_
		D_in_pad[7]/U0/U1:YIN	net	D_in_pa	ad[7]/U0/N	VET1		+	0.000	0.898	r	_
		D_in_pad[7]/U0/U1:Y	cell				ADLIB:IOIN_IB	+	0.032	0.930	1 r	_
		DataD[7]:D	net	D_in_c[7]			+	2.643	3.573	r	_
		data arrival time								3.573		_
		.										
		Data required time co	E dame d Octor Octor duriet						0.500	0.500		_
		Deter DITL OF K	External Setup Constraint						2.500	2.500	_	-
	\vdash	DataD[7]:CEK	Library actus time					-	1.732	4.232	r	_
		DataD[7]:D	Library setup time				ADUB: DENTICU	-	0.402	3.030		
	⊢⊦	data required time				I				2 0 0 0 1		

- External Setup Check Calculation
 - Arrival time = Launch edge (0) + max input delay + max Data path
 - Required time = External Setup + min Clock to FF1 Setup of FF1
 - Slack = Required Arrival = Violation if < 0</p>



SmartTime Clock to Output Check

 Clock to Output is Displayed in the Maximum Delay Analysis View for Each Clock Domain



- Clock to Output Calculation
 - Arrival time = Launch edge (0) + max Data path
 - Required time = Capture edge (T)
 - Slack = Required Arrival = Violation if < 0



Clock to Output Check w/ Output Delay Constraint

Enter Constraint as Output Delay





Clock to Output w/ Output Delay Constraint

ay Analysis	View	1							
i	From	*			To *				
					Apply	Filter	Store Fi	lter R	eset Filter
	1	Source Pin	Sink Pin	Delay (ns) A Slac	k (ns) Arrival (ns) Requ	uired (ns	Clock to	Out (ns)	
1	1	reg3/U0:CLK	У	3.932 -	0.980 6.980	6.000)	6.980	
o Register		Pin Name	Туре	Net Name	Cell Name	Op I	Delay (ns)	Total (ns)	Fanout E
utput 1		From: reg3/U0:CLK							
2		То: у						100,000-00	
ut 3		data required time						6.000	
4		data arrival time				-		6.980	
5		slack						-0.980	
6	T								
		Data arrival time ca	lculation						
7		clk1					0.000	0.000	
8		reg3/U0:CLK	clock network		and a state of the	+	3.048	3.048	r
9	1	reg3/U0:Q	cell		ADLIB:DFEG	+	0.661	3.709	1 f
1	0	outbugy1/U0/U3:A	net	s7		+	0.245	3.954	f
1	1	outbugy1/U0/U3:Y	cell		ADLIB:IOOE_BUFF	+	0.035	3.989	1 f
1	2	outbugy1/U0/U1:A	net	outbugy1/U0/NET3		+	0.000	3.989	f
1	3	outbugy1/U0/U1:Y	cell		ADLIB:IOFIFO_OUTBUF	+	0.031	4.020	1 f
1	4	outbugy1/U0/U0:D	net	outbugy1/U0/NET1		+	0.000	4.020	f
1	5	outbugy1/U0/U0:PAD	cell		ADLIB:IOPAD_TRI	+	2.960	6.980	0 f
1	6	y	net	У		+	0.000	6.980	f
1	7	data arrival time						6.980	
1	8								
		Data required time of	calculation						
1	9	clk1	Clock Constraint				10.000	10.000	
2	0	y State	Output Delay Constraint			2	4.000	6.000	
1 2	1		•					6.000	

- Setup Check
 - Arrival time = Launch edge (0) + max Data path
 - Required time = Capture edge (T) Output Delay
 - Slack = Required Arrival = Violation if < 0</p>



Adding Timing Exceptions

False Path Example

Multiplexer S Input Never Changes

• FF1, FF2 and FF3 to FF4 through MX0:A are False Paths




SmartTime Maximum Frequency

SmartTime [FALSE_PATHS *	*] - [Maximum Delay Analysis View]	
<u>≩ Fi</u> le Edit ⊻iew <u>A</u> ctions <u>T</u> ools	: <u>W</u> indow <u>H</u> elp	_ 8 ×
Summary Summary S Datasheet CLK Register to Register External Setup Clock to Output Register to Asynchron External Recovery Asynchronous to Regi Synchronous to Regi Input to Output Summary User Sets	Design: FALSE_PATHS Family: ProASIC3 Max Operating Condition: WORST Die: A3P060 Min Operating Condition: BEST Package: 100 VQFP Voltage: COM Temperature: COM Design State: Post-Layout Speed Grade: -F Using Enhanced Min Delay Analysis State: Period (period (ns) Frequency (MH2) Required Period (ns) Frequency (MH2) Setup (ns) Hold (ns) to Out (ns)	
	I/O Details: Name Min Delay (ns) Max Delay (ns)	
•	Input to Output N/A N/A	✓
Ready	Temp: COM Volt: C	IOM Speed: -F 🏼 🎵



SmartTime *Timing Analysis*

SmartTime [FALSE_PATHS *] - [N	laximum Delay Analysi	s View]								(
<u> F</u> ile <u>E</u> dit <u>V</u> iew <u>A</u> ctions <u>T</u> ools	<u>W</u> ine	dow <u>H</u> elp										- 8 ×
	20	<u>></u>	8	😏 🕅 🐜 🖏	🗞 🛛	2.2	fr					
MAX	Fron	n / *				T	o *				4	
🖃 ୍ଦ୍ରି Summary								A	pply Filter	Store Filter	r Re	set Filter
⊡ <mark>&</mark> Datasheet ⊡ × @ CLK		Source Pin		Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)	
Register to Register	1	FF1:CLK	FF4:D		3.788	-0.114	6.616	6.502	0.856	4.992	0.348	
External Setup	2	FF0:CLK	FF4:D		3.129	0.072	6.430	6.502	0.856	4.806	0.821	
Clock to Dutput	3	FF3:CLK	FF4:D		3.280	0.079	6.423	6.502	0.856	4.799	0.663	
Hegister to Asynchron	4	FF2:CLK	FF4:D		3.613	0.191	6.311	6.502	0.856	4.687	0.218	
External Recovery						/						
Asynchronous to Hegi						/						
E Pin to Pin		Pin Name		Tune	N	t Name	L Cel	I Name	On Dela	u (ns) Total (ns	Eanout	t Edgel 🔨
Input to Uutput	1			Турс	/							
Ser Sets	<u> </u>	To: FF4.D										
		data required time								6.50	2	
		data arrival time						-		6.61	6	
		slack			1					-0.11	4	
۱		D-1			7							~
Ready	-				/					Temp: COM Vol	t: COM S	peed: -F 🏼 🏑
				/								

Timing Violation



Timing Analysis Expanded Path

🕑 s	martTime [FALSE_PATHS *] -	[Maximum Delay	- Expanded Path V	/iew: FF1:CLK ->	FF4:	D]			
🥋 E	ile <u>E</u> dit <u>V</u> iew <u>A</u> ctions <u>T</u> ools <u>V</u>	<u>V</u> indow <u>H</u> elp							_ @ :
6	s Re FX 9	<u> </u>	<u> </u>	n 🙀 🐉	<u>.</u>	× 🕅 😭			
	Pin Name	Туре	Net Name	Cell Name	Ор	Delay (ns)	Total (ns)	Fanout Edge	2
1	From: FF1:CLK								
	To: FF4:D								
	data required time					ļ	6.502		
	data arrival time				•	ļ	6.616		
	slack						-0.114		
	Data arrival time calculation								
						0.000	0.000		
		Clock source			+	0.000	0.000	r	
	CLK_pad/U0/U0:PAD	net	CLK		+	0.000	0.000	r	
	CLK_pad/U0/U0:Y	cell		ADLIB:IOPAD_IN	+	1.202	1.202	1 r	
	CLK_pad/U0/U1:YIN	net	CLK_pad/U0/NET1		+	0.000	1.202	r	
	CLK_pad/U0/U1:Y	cell		ADLIB:IOIN_IB	+	0.052	1.254	5 r	
	FF1:CLK	net	CLK_c		+	1.574	2.828	1	
		-80							
<									>
Ready	,								Temp: COM Volt: COM Speed: -F

This is a false path



SmartTime Entering False Path Exceptions

SmartTime [FALSE_PATHS *]	- [Max	cimum Delay Analy	sis View]								
À File Edit View Actions Tools	Window	v Help										_ 8 ×
	2	<u>></u>	2	<u> 🦄 🐜</u>	• ¥ø 🖄	<u>۳ א</u>	fr 🎐					
	From	*				т	·o *					
MAX Picht								A	pply Filter	Store Filte	r Re	eset Filter
Mouse		Source Pin		Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)	
Click!	1		ICC4.D		3.788	-0.114	6.616	6.502	0.856	4.992	0.348	
	$\frac{2}{2}$	riot			3.129	0.072	6.430	6.502	0.856	4.806	0.821	-
Begister	<u>3</u> -	100			3.280	0.079	6.423	6.502 C 502	0.855	4.799	0.563	
Evternal	4 A	dd False Path Constrain	it		3.613	0.191	6.311	6.002	0.606	4.667	0.218	
Asynchri egi	A	dd Max Delay Constrair dd Multicycle Path Cons	it itraint									
				e Net	Name	Cell	Name	Op Delay ([ns] Total	l (ns) Fanout I	Edge	~
Set Sets		xpand selected paths ross-probe selected pat	:hs									
	da	ata required time							1	6.502		
	da	ata arrival time						-	1	6.616		
	si	ack							-	0.114		
↓												~
Create a new false path constraint										Temp: COM Vo	lt: COM S	Speed: -F 🏼 🎵



Add False Path Exception

False Path Constraint Through MX0:A





SmartTime Maximum Frequency with False Paths





SmartTime Expanded Path Timing Information

 Right-click a Path in the Path List Displays the Expanded Path in a Separate Window

≽ Maximum Delay An	nalys	is View								. 🗆 🗙
	From	*			То	* A	pply Filter	Store Filt	er R	eset Filter
Register to Register		Source Pin	s	ink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minin 🔨 Perioc
Clock to Output	1 2 3 4 4 1 2 3	Copy Print Add False Path Constrain Add Max Delay Constrain Add Multicycle Path Cons Expand selected paths Cross-probe selected pa	oritition nt straint ths	pe	4.744 4.725 4.711 4.647 4.509	0.568 0.606 0.621 0.676 0.734	6.543 6.524 6.510 6.446 6.207 et Name	7.111 7.130 7.131 7.122 7.124	0.402 0.376 0.402 0.276	Cell Na A



SmartTime Expanded Path (cont.)

Expanded Path View Includes a Schematic of the Path

	Pin Name	Туре	Net Name	Cell Name	0p	Delay (ns)	Total (ns)	Fanout	E
	From: Q[0]:CLK		4			,			
	To: Q[11]:D								
	data required time						7.111		Т
	data arrival time				-		6.543		t
	slack						0.568		t
	Data arrival time calculation								
	СГК					0.000	0.000		Т
	Q[0]:CLK	clock network			+	1.799	1.799		r
	Q[0]:Q	cell		ADLIB:DFN1C1	+	0.535	2.334	4	f
0	COUNTING_count_3_G_1_5:A	net	Q_c[0]		+	0.655	2.989		f
1	COUNTING_count_3_G_1_5:Y	cell		ADLIB:NOR2B	+	0.380	3.369	6	f
2	COUNTING_count_3_G_1_3:B	net	COUNTING_count_3_DWACT_ADD_CI_0_tmp[0]		+	0.288	3.657		f
3	COUNTING_count_3_G_1_3:Y	cell		ADLIB:NOR3B	+	0.458	4.115	3	f
4	COUNTING_count_3_I_82:A	net	COUNTING_count_3_DWACT_ADD_CI_0_g_array_3[0]		+	0.364	4.479		f
5	COUNTING_count_3_I_82:Y	cell		ADLIB:NOR2B	+	0.380	4.859	2	f
6	COUNTING_count_3_I_61:A	net	COUNTING_count_3_DWACT_ADD_CI_0_g_array_11_1[0]		+	0.760	5.619		f
7	COUNTING_count_3_I_61:Y	cell		ADLIB: AX1C	+	0.719	6.338	1	f
8	Q[11]:D	net	COUNTING_count_3[11]		+	0.205	6.543		f
9	data arrival time						6.543		
0	Data required time calculati	ion							
1	СГК	Clock Constraint				5.714	5.714		
2		clock network			+	1.799	7.513		r
3	Q[11]:D	Library setup		ADLIB:DFN1C1	-	0.402	7.111		
4	data required time						7.111		

Right click in window to zoom



Timing Analysis with SmartTime

- Design Summary
- Maximum Delay Analysis View
- Minimum Delay Analysis View
- Cross Clock Domain Analysis
- Removal and Recovery Checks
- SmartTime Scenarios



Minimum Delay Analysis View Register to Register Path Set

Identify Internal Hold Violations





SmartTime Hold Check

Hold Check is Displayed in the Minimum Delay Analysis View



- Arrival time = Launch edge (0) + min Clock to FF1 + min Data path
 - Required time = Launch edge (0) + max Clock to FF2 + Hold of FF2
 - Slack = Arrival Required = Violation if < 0



SmartTime Hold Check (cont.)

Minimum Delay Analysis View											
\frown	From	*			То	*					
		,									
							Ap	ply Filter	Stor	e Filter	Reset Fill
🖓 Summary 📃											
Register to Register		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Hold (ns)	Skew (ns)		
External Hold	1	g2_2_l2/l1/current_state[15] g2_	_2_I2/I1/current_state[[14] 0.491	0.458	1.829	9 1.37	1 0.000	0.03	3	
Electric Dulput		:CLK :D									
Register to Register			A 10447	241 0 400		4 000	1 4 AZ				
External Hold		Pin Mame	Туре	Ne	Name		cell Name	OD D	elay (ns)	rotai (ns)	Fanout
Clock to Output	1	From: g2_2_l2/l1/current_stat	te[15]:CLK								
⊡ ✓ @ clock_20	2	10: g2_2_12/11/current_state[/	14]:U							4 000	
Register to Register	3 4	data arrival time								1.029	
External Hold	5	slack						-		0.458	
Clock to Output	5 1	Sidek								0.400	
		Data arrival time calculation									
Register to Register	7	clock 160							0.000	0.000	
External Hold	8	 a2_2_l2/11/current_state[15]:CLk	C clock petwork					+	1 338	1 338	r
Charles Contactor	-	gr_r_ierus	CIOCKTICLWOIR					· ·	1.5501	1.000 [
Clock to Output	9	g2_2_l2/l1/current_state[15]:Q	cell			AD	LIB:DFN1C0	+	0.306	1.644	1 r
Clock to Output	9 10	g2_2_12/11/current_state[15];Q g2_2_12/11/current_state[14];D	cell	g2_2_l2/l1/cu	rent_state[AD	DLIB:DFN1C0	+ +	0.306	1.644	1 r
Clock to Output □	9 10 11	g2_2_12/11/current_state[15]:Q g2_2_12/11/current_state[14]:D data arrival time	cell net	g2_2_l2/l1/cu	rent_state[AD	LIB:DFN1C0	+ +	0.306	1.644 1.829 1.829	1 r
Clock to Output □	9 10 11 12	g2_2_12/11/current_state[15]:Q g2_2_12/11/current_state[14]:D data arrival time	cell net	g2_2_l2/l1/cu	rent_state[AC 15]	DLIB:DFN1C0	+	0.306	1.644 1.829 1.829	1 r r
Clock to Output □	9 10 11 12	g2_2_12/11/current_state[15]:Q g2_2_12/11/current_state[14]:D data arrival time Data required time calculatio	cell net	g2_2_l2/l1/cu	rrent_state[AC 15]	DLIB:DFN1C0	+	0.306	1.644 1.829 1.829	1 r
Clock to Output □	9 10 11 12 13	g2_2_12/11/current_state[15]:Q g2_2_12/11/current_state[14]:D data arrival time Data required time calculatio clock_160	cell net	g2_2_l2/l1/cu	rrent_state[A[15]	DLIB:DFN1C0	+ +	0.306	1.644 1.829 1.829 0.000	1 r
Clock to Output g2_1_l2/l1/sclock_cld External Hold Clock to Output Clock to Output g2_4_l2/l1/sclock_cld Register to Register External Hold	9 10 11 12 13 14	g2_2_12/11/current_state[15]:Q g2_2_12/11/current_state[15]:Q data arrival time Data required time calculatio clock_160 g2_2_12/11/current_state[14]:CLK	cell net Clock Constraint Clock Constraint	g2_2_l2/l1/cu	rrent_state[AE	DLIB:DFN1C0	+ · · · · · · · · · · · · · · · · · · ·	0.306 0.185 0.000 0.000 1.371	1.644 1.829 1.829 0.000 1.371	1 r r r
Clock to Output g2_1_l2/l1/sclock_cld External Hold Clock to Output g2_4_l2/l1/sclock_cld Register to Register External Hold Clock to Output	9 10 11 12 13 14 15	g2_2_12/11 /current_state[15]:Q g2_2_12/11 /current_state[14]:D data arrival time Data required time calculatio clock_160 g2_2_12/11 /current_state[14]:CLK g2_2_12/11 /current_state[14]:D	clock forwork net Clock Constraint Clock Constraint Clock network Library hold	g2_2_l2/l1/cu	rrent_state[AE 15]	DLIB:DFN1C0	+ + + + +	0.306 0.185 0.000 1.371 0.000	1.833 1.644 1.829 1.829 0.000 1.371 1.371	1 r r

Hold Check

- Arrival time = Launch edge (0) + min Clock to FF1 + min Data path
- Required time = Capture edge (0) + max Clock to FF2 + Hold of FF2
- Slack = Arrival Required = Violation if < 0



SmartTime External Hold Check

- External Hold Defines the Timing Requirements at the Input Pins
- External Hold Check is Displayed in the Minimum Delay Analysis View for Each Clock Domain





- External Hold Check Calculation
 - Arrival time = min Input Pad to FF1
 - Required time = max Clock to FF1 + Hold of FF1
 - External Hold = Arrival Required



SmartTime External Hold Check

3	🧲 Minimum Delay Analysis	View								>		
	\mathbf{s}	From	*			To *						
	min ⊡-⊗ Summary						Apply F	Filter Store Fi	lter	Reset Filter		
	⊡⊶ Y @0 dk1		Source Pi	in	Sink Pin	Delay Slack	Arr	rival Required	Hold (ns)	External Hold (ns)	T	
	Register to Register External Hold	1	а	reg1/U	0:D	1.208		1.208	0.000	0.890		
	Clock to Output		Pin Name	Туре	Net Name	Cell Name	Ор	Delay (ns) Tota	(ns) Fa	nout Edge		
	Input to Output	1	From: a To: reg1/U0:D									
	Ser Sets	3	data arrival time						1.208			
		4	data required time				-		N/C			
		5	slack						N/C			Slack cannot be
		6										
			Data arrival time	calculation								calculated if clock
		7	а					0.000	0.000	f		constraint is not
		8	inbuga/U0/U0:PAD	net	а		+	0.000	0.000	f	Χ	constraint is not
		9	inbuga/U0/U0:Y	cell		ADLIB:IOPAD_IN	+	1.016	1.016	1 f		entered
		10	inbuga/U0/U1:A	net	inbuga/U0/NET1		+	0.000	1.016	f		cifici cu
		11	inbuga/U0/U1:Y	cell		ADLIB:IOFIFO_INBUF	+	0.023	1.039	1 f		
		12	inbuga/U0/U2:A	net	inbuga/U0/NET2		+	0.000	1.039	f		
		13	inbuga/U0/U2:Y	cell		ADLIB:IOI_BUFF	+	0.024	1.063	1		
		14	reg1/U0:D	net	s1		+	0.145	1.208	f		
		15	data arrival time						1.208			
		16	Defense in the	1								
		47	Data required tin	ne calculation				NIC	AL/C			
		1/	CIK1	ala ak a atu sala				N/C	W/C			
	4	19	reg1/U0:0LK	Library hold		ADI IB:DEEG	+	2.090	N/C			
		<u> </u>	reg nee.b	cionary noid	1	Accession co		0.000				

External Hold Check – Minimum Delay Analysis View

- Arrival time = min Input Pad to FF1
- Required time = max Clock to FF1 + Hold of FF1
- Slack = Arrival Required = Violation if < 0



Timing Analysis with SmartTime

- Design Summary
- Maximum Delay Analysis View
- Minimum Delay Analysis View
- Cross Clock Domain Analysis
- Removal and Recovery Checks
- SmartTime Scenarios



SmartTime Cross-Clock Domains



- SmartTime Performs Setup Check Across Clock Domains
 - SmartTime Looks at the Relationship Between the Active Clock Edges Over a Full Repeating Cycle, Equal to the Least Common Multiple of the Two Clock Periods
 - For Each Capture Edge at the Destination Flip-flop, SmartTime Assumes That the Corresponding Launch Edge Is the Nearest Source Clock Edge Occurring Before the Capture Edge



SmartTime

Cross-Clock Domain Analysis Activation

- Activate Cross-clock Domain Analysis for a Particular Clock Domain
 - SmartTime Automatically Detects All Other Clock Domains With Paths Ending at Selected Clock Domain

SmartTime Options	
Smart Lime Options Option Categories Select a category: General Analysis View Advanced	General Operating Conditions Perform maximum delay analysis based on Perform minimum delay analysis based on BEST Clock Domains Clock Domains Include inter-clock domains in calculations for timing analysis. Image: The perform and removal checks.
Help	Restore Defaults OK Cancel



SmartTime Cross-Clock Domains in SmartTime

Inter clock domain analysis





Timing Analysis with SmartTime

- Design Summary
- Maximum Delay Analysis View
- Minimum Delay Analysis View
- Cross Clock Domain Analysis
- Removal and Recovery Checks
- SmartTime Scenarios



Removal/Recovery Checks

- Definition
 - An asynchronous signal should not be de-activated around the active clock edge



- Recovery needs to be checked in Max delay analysis
- Removal needs to be checked in Min delay analysis



Removal/Recovery Checks: Analysis

≽ Maximum Delay Analysis View	,									
	From	*			То *					
MAX						Ap	ply Filter	Store	Filter Res	et Filter
□ · · · · · · · · · · · · · · · · · · ·		Source Pin	Sink Pin	Delay S (ns) (Slack Arrival ns) (ns)	Req (uired Re ns)	covery (ns)	Minimum Period (ns)	Skew (ns)
External Setup	1	regrst:CLK I	reg2:CLR	1.336	2.688 3.10	7	5.795	0.222	2.312	0.754
Clock to Output	2	regrst:CLK	reg1:CLR	1.279	3.061 3.05	0	6.111	0.222	1.939	0.438
Asynchronous to Register		Pin Name	Туре	Net Nan	ne Cell Name	On	Delay (ns)	Total (n	s) Fanout Ede	1e
Register to Asynchronous	1	From: regrst:CLK	.,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,			- P	2014) (110)			<u>, -</u>
External Recovery	<u> </u>	To: reg2:CLR								
E Pin to Pin		data required time						5.79	15	_
Input to Output		data arrival time				-		3.10)7	
		slack						2.68	8	
		Data arrival time calculatio	n							
		clock					0.000	0.00	0	
		regrst:CLK	Clock network			+	1.771	1.77	11 r	
		regrst:Q	cell	_	ADLIB:DFN1C0	+	0.434	2.20)5 2 r	_
		reg2:CLR	net	synreset	t	+	0.902	3.10)7 r	_
		data arrival time						3.10)7	_
		Data required time calcula	tion							
		clock	Clock Constraint				5.000	5.00	0	
		reg2:CLK	Clock network			+	1.017	6.01	7 r	
		reg2:CLR	Library recovery time		ADLIB:DFN1C0	-	0.222	5.79	15	
•		data required time						5.79	95	



Timing Analysis with SmartTime

- Design Summary
- Maximum Delay Analysis View
- Minimum Delay Analysis View
- Cross Clock Domain Analysis
- Removal and Recovery Checks
- SmartTime Scenarios



SmartTime Scenarios

- Create constraint options for testing
 - Use for pre-layout timing
 - Use to drive TDPR
- Launch from Tools => Constraints Editor => New Scenario





SmartTime Scenarios

- Brings up Timing Constraints Dialog = "Scenario_1"
 - Additional Scenarios can be created
- Use Constraints Wizard to Enter Constraints
 - Wizard adds constraints only to the active scenario
- Import SDC or Export Scenario with SDC
- Scenarios can be Added, Edited, Deleted, Copied

SmartTime [counter16 *]		
File Edit View Actions Tools Win	ndow Help	
	22 🔀 🐵 🛪 🖉 😏 🏧 🐃 🛸 🔉 🖄 🔛 🙄 💟	
Scenario_1 Scenario_2 Scenario_3	Constraints Editor for scenario Scenario_1 Constraints Editor for scenario Scenario_2 Constraints Editor for scenario Scenario_3 Constraints Constraints Constraints Syntax Period Frequency Dutycycle First Clock Generated Clock Generate	et Waveform File Comments



SmartTime Scenarios

Use Options => Advanced => Scenarios

- Use specific scenario for timing analysis
- Use specific scenario for TDPR

SmartTime Options		×
Option Categories 	Advanced Special Situations Use loopback in bi-directional buffers (bibufs) Break paths at asynchronous pins Disable non-unate arcs in clock network Scenarios Use this scenario for timing analysis: Primary Use this scenario for timing-driven place-and-route: Primary Scenario_1 Scenario_2	
Help	OK Cancel	



SmartTime Timing Reports

SmartTime *Timing Reports*

- SmartTime Can Generate Five Types of Reports:
 - Timing Report
 - Timing Violation Report
 - Data Sheet Report
 - Bottle Neck Report
 - Constraints Coverage
 - Combinational Loops



SmartTime Timing and Timing Violation Reports

SmartTime [find_min] - [Minimum Delay Analysis View]			
<u> File</u> Edit View Actions	Tools Window Help		
	Constraints Editor Constraint Wizard Timing Analyzer Constraint Checker	▶ <u>₩ ≍ 2 97 m ma ba</u>	
	Reports	 Report Paths 	
	Options	Report Violations Report Datasheet Report Bottlenecks Report Constraints Coverage	
		Report Combinational Loops	

Timing Report Contains Timing Information of the Design in a Text Format

- Information Can Be Customized
- Timing Violation Report Contains a Flat List of Paths With Timing Violations (No Breakdown by Clock Domain).



SmartTime Timing Report Options

Timing Report Options		×
Option Categories - Select a category: - General - Paths - Sets - Clock Domains	Format Plain Text Comma Separated Values Summary Include a gummary of timing results in this report Analysis Use Magimum Delay Analysis Use Migimum Delay Analysis Slack Filter paths by slack threshold Maximum slack to include: Ins Eestore Default 	
Help	OK Cancel	



SmartTime Timing Report Options

Paths & Sets Options

• Include User Defined Sets in Timing Report

SmartTime Timing Report Options

- Clock Domains
 - Specify Clock Domains to be Included in the Timing Report

Option Categories Clock Domains Paths Sets Clock Domains Limit reporting on clock domains to specified domains Clock Domains Select Domains	ming Report options		
	Option Categories Report Options General Paths Sets Clock Domains	Clock Domains Display of Clock Domains Limit reporting on clock domains to specified domains Clk2 Clk1 Select Domains Restore Defe	ults



SmartTime Timing Report Structure

- Header
 - Design Information, Operating Conditions...
- Summary
 - Data-sheet (Freq, ext setup/hold, min/max clock-to-out...)
- Clock Domain Details
 - Path Sets (reg2reg, in2reg, reg2out, Custom...)
 - Path Details
 - Expanded Paths
- Inter-clock Domain Details
- Pin-to-pin Path
 - Path Sets (in2out, Custom...)



SmartTime *Timing Report*

🔁 COUNT16 - Timing Report		
<u> Eile A</u> ctions <u>H</u> elp		
Timing Report Max Delay Ana SmartTime Version 3.0 Actel Corporation - Actel D Copyright (c) 1989-2007 Date: Wed Mar 14 22:07:32 2	lysis esigner Software Release v7.3 SP1 (Version 7.3.1.9 007	9)
Design: COUNT16 Family: ProASIC3 Die: A3P060 Package: 100 VQFP Temperature: COM Voltage: COM Speed Grade: -2 Design State: Pre-Layout Min Operating Condition: BE Max Operating Condition: WO Using Enhanced Min Delay An	ST RST alysis	
SUMMARY		
Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns): Max Clock-To-Out (ns):	CLK 5.884 169.952 5.714 175.009 4.234 0.010 2.158 6.320	
Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns):	CLKA N/A N/A 5.000 200.000 N/A N/A N/A	



SmartTime

Timing Violations Report Options

- General Options
 - Specify Maximum or Minimum Delay Analysis
 - Enter Slack Threshold

Timing Violations Repo	rt Options	X
Option Categories → Select a category: → General → Paths	Analysis • Use Magimum Delay Analysis • Use Minimum Delay Analysis Slack Slack ✓ Filter paths by slack threshold Maximum slack to include: ① Pestore Defa	aults
Help	OK Cancel	



SmartTime Timing Violations Report Options

- Path Options
 - Limit Number of Reported Paths

Timing Violations Repo	rt Options	×
Option Categories	Paths	
Select a category: General Paths	Display of paths Limit the number of reported paths Limit the number of reported paths per section to: Imit the number of expanded paths per section to: Imit the number of expanded paths per section to: Imit the number of expanded paths per section to:	ults
Help	OK Cancel	



SmartTime Timing Violation Report Structure

- Header
 - Design Information, Operating Conditions...
- Paths
 - List of Paths With Timing Violations


SmartTime Timing Violation Report

🛚 COUNT16 - Timing_violati	ions Report		×
<u>File A</u> ctions <u>H</u> elp			
Timing Violation Report Max De	lay Analysis		^
Timer Version 2.0			
Actel Corporation - Actel Desig	gner Software Release 6.2 (Version 6.2.0.23)		
Copyright (c) 1989-2005			≡
Date: Ide May 31 15:00:43 2003			
Design: COUNT16 Femilu: Pro/SIC3		l	-
Die: A3P060			
Package: 100 VQFP			
Temperature: COM			
Voltage: COM			
Speed Grade: -2			
Design State: Post-Layout			
Min Operating Condition: BEST			
Max Operating Condition: WORST			
Path 1			
From:	Q[8]:CTK		
To:	Q(8)		
Delay (ns):	5.048		
Slack (ns):	-2.382		
Arrival (ns):	6.846		
Required (ns):	4.464		
Path 2			
From:	Q[11]:CLK		
To:	Q(11)		
Delay (ns):	4.774		
Slack (ns):	-2.109		
Arrival (ns):	6.573		
Required (ns):	4.464		v
		>	



SmartTime Datasheet Report

- Content
 - Pin Description
 - Pin location on the package
 - Port name
 - Type (input, output, inout, clock)
 - I/O Technology used
 - DC Timing Characteristics
 - Electrical parameters of each I/O technology (slew, output load month of the second loops... voltages,)
 - AC Timing Characteristics
 - External Timing Requirements
- New analysis view in the SmartTime Analyzer
- Report Format
 - Text format or CSV (Comma Separated Value)





Datasheet Report AC Timing Characteristics

- Maximum Clock Frequency for all External Clocks
- External Setup/Recovery/Hold/Removal for Each Input Port with Respect to External Clocks
- Clock-to-out for Output Ports
- Input-to-Output for Combinational Paths



Datasheet Report

Pin Descr	ripti	on							
Name	Loc	ation	Type	Techno	+				
<pre> a[0] b[0] reset ci clk y[0] co en ++ DC Electr ++</pre>	J14 H15 K1 B8 R7 C9 B7 L2 	Charac	Input Input Input Input Clock Output Output Input +	LVCMOS15 LVCMOS25 SSTL2I LVTTL (1 GTLP25 LVTTL (2 LVTTL (3 PCI	+ 	+	+	+	
Name		Vcci (V)	Resistor Pull 	Input Delay 	Hot Swappable 	Vccr (V) 	Output Drive (mA)	Slew 	Output Load
+	15 25 1) 22) 3)	2.5 1.5 2.5 3.3 3.3 3.3 3.3 3.3 2.5	Up Up None None None None	no no no no no no	yes yes yes yes yes yes no yes	1	 24 12 	 Low High 	35 40



Datasheet Report (cont.)

 .k .k 0] 0]	before before	 clk (rise) clk (rise)	Min 	Max + 189.143 	Unit ++ MHz ns ns
.k .k 0] 0]	before before	 clk (rise) clk (rise)	 5.287 -0.946 -2.642	189.143 	MHz ns ns
k 0] 0]	before before	 clk (rise) clk (rise)	5.287 -0.946		ns ns
0]	before before	clk (rise) clk (rise)	-0.946		ns
0]	before	clk (rise)	-2.642	1	1 1
i		. ,	1 2.012		ns
-	before	clk (rise)	-3.100		ns
eset	before	clk (rise)	-0.096		ns
0]	after	clk (rise)	-1.278		ns
0]	after	clk (rise)	-2.062		ns
.	after	clk (rise)	-2.241		ns
eset	after	clk (rise)	-0.429		ns
eset	before	clk (rise)	-0.266		ns
eset	after	clk (rise)	-0.429		ns
.k (rise)	to	co	3.545	7.420	ns
.k (rise)	to	y[0]	6.720	14.309	ns
	set 0] 0] set set set k (rise) k (rise)	before set before 0] after 0] after after set after set before set after k (rise) to k (rise) to	before clk (rise) set before clk (rise) 0] after clk (rise) 0] after clk (rise) after clk (rise) set after clk (rise) set before clk (rise) set after clk (rise) k (rise) to co k (rise) to y[0]	before clk (rise) -3.100 set before clk (rise) -0.096 0] after clk (rise) -1.278 0] after clk (rise) -2.062 after clk (rise) -2.241 set after clk (rise) -0.429 set before clk (rise) -0.266 set after clk (rise) -0.429 k (rise) to co 3.545 k (rise) to y[0] 6.720	before clk (rise) -3.100 set before clk (rise) -0.096 0] after clk (rise) -1.278 0] after clk (rise) -2.062 after clk (rise) -2.241 set after clk (rise) -0.429 set before clk (rise) -0.266 set after clk (rise) -0.429 k (rise) to co 3.545 7.420 k (rise) to y[0] 6.720 14.309



SmartTime Bottleneck Report

SmartTime [find_min]	- [Minimum Delay A	nalysis View]
≲ File Edit View Actions	Tools Window Help	
	Constraints Editor Constraint Wizard Timing Analyzer Constraint Checker	• <u>• × 2 </u> <u>• *</u>
	Reports	Report Paths
	Options	Report Violations Report Datasheet Report Bottlenecks Report Constraints Coverage
		Report Combinational Loops

- Bottleneck Analysis
 - A bottleneck is a point in the design that contributes to multiple failing paths
 - SmartTime finds and lists all bottlenecks according to severity
- SmartTime "Bottleneck Analysis Report" Shows
 - Severity: "Path_Costs"
 - Lists instances causing the greatest amount of delay
 - Reports total max delay caused by the instance
 - # of Occurrences: "Path_Count"
 - Lists instances causing greatest number of path violations
 - Reports number of paths affected by the instance delay



Bottleneck Analysis Report General Options

- Format
 - Text or CSV
- Maximum or Minimum Delays
 - Default uses Max Delay
- Filter by Slack Value
 - Violations below the specified value are not reported
 - Default = 0 ns

Timing Bottleneck Report Options		2
Option Categories	General	
⊡-Select a category: General Bottleneck Sets	Format © Plain Text © Comma Separated Values	
	Analysis © Use Maximum Delay Analysis © Use Minimum Delay Analysis	
	Slack ✓ Filter paths by slack threshold	
	Maximum slack to include: 0 ns	
	Restore Defau	lts
Help	OK Cancel	



Bottleneck Analysis Report Bottleneck Options

- Cost Type
 - Path Count
 - Combined Delay
- Specify
 - Number of Paths to Analyze
 - Number of Parallel Paths per Section
 - Number of Instances

Timing Bottleneck Report Option		×
Option Categories	Bottleneck	
⊟- Select a category: General Bottleneck Sets	Bottleneck options	
	Limit the number of paths per section to:	
	Limit the number of parallel paths per section to:	
	Limit the number of reported instances to: 10	
	Restore Defa	ults
Help	OK Cancel	



Bottleneck Analysis Report Set Options

- Define Sets to be Analyzed:
 - Entire Design
 - Specific Clock Domain
 - User Defined Set
- Report Instances on Violating Paths
 - From starting from location
 - To a destination location

Timing Bottleneck Report Options	
Option Categories	Sets
⊡-Select a category: General Bottleneck Sets	Set Selection © Entire Design © Clock Domain Clock: Type: Type: © Use existing User Set Name: Filter From: To: Dectore Defaultr
Help	OK Cancel



Bottleneck Analysis Path Count Report

- Path Count Report Shows:
 - Number of paths where an instance is causing delay
 - The corresponding instance name





Bottleneck Analysis Path Cost Report

Lists total combined Max Delay caused by an instance





SmartTime Constraint Coverage Report

SmartTime [find_min]	- [Minimum Delay A	nalysis View]
<u> File Edit</u> View Actions	Tools Window Help	
	Constraints Editor Constraint Wizard Timing Analyzer Constraint Checker	▶ <mark>@ ≍ ⊘ ೨ ‰ ‱ छ</mark> ▶ *
	Reports	Report Paths
	Options	Report Violations Report Datasheet
port		Report Bottlenecks Report Constraints Coverage Report Combinational Loops

Constraint Coverage Report

- Reports statistics of constraints
 - Met
 - Not Met
 - Not Tested



Constraint Coverage Report

ile Actions Help	ms_coverage Re	ponc			
SmartTime Versio					
Actel Cornoratio	n 5.0 n - Actel Des	igner Software	e Release v8.2	Wersion 8.3	2.0.17)
		igner sorosari			,
Design		find min			
Family		ProASIC3			
Die		A3P125			
Package		208 PQFP			
Temperature		COM			
Voltage		COM			
Speed Grade		-2			
Design State		Post-Layout	5		
Analysis Min Ca	se	BEST			
Analysis Max Ca	se	WORST			
Scenario for Ti	ming Analysis	Primary			
Using Enhanced	Min Delay Ana	lysis			
Coverage Summary					
	+	+	L	L	±
Type of check	Met	Violated	Untested	Total	т
	+	+	+	+	+
Setup	219	23	5	247	l
Recovery	0	0	175	175	I
	24	0	0	24	I
Output Setup					
Output Setup Total Setup	243	23	180	446	l
Output Setup Total Setup Hold	243 242	23 0	180 5	446 247	
Output Setup Total Setup Hold Removal	243 242 0	23 0 0	180 5 175	446 247 175	
Output Setup Total Setup Hold Removal Output Hold	243 242 0 24	23 0 0	180 5 175 0	446 247 175 24	
Output Setup Total Setup Hold Removal Output Hold Total Hold	243 242 0 24 24	23 0 0 0	180 5 175 0 180	446 247 175 24 446	
Output Setup Total Setup Hold Removal Output Hold Total Hold	243 242 0 24 266	23 0 0 0	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold	243 242 0 24 266	23 0 0 0	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold 	243 242 0 24 266 +	23 0 0 0	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold 	243 242 0 24 266 +	23 0 0 0	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold Conhancement Sugg	243 242 0 24 266 +	23 0 0 0	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold Chhancement Sugg Clock domain: mc - Input delay in	243 242 0 24 266 +	23 0 0 0 +	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold Conhancement Sugg Clock domain: mc - Input delay in STROBEn, mrst	243 242 0 24 266 +	23 0 0 0 +	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold Contain Hold Clock domain: mc - Input delay in STROBEn, mrst	243 242 0 24 266 +	23 0 0 0 +	180 5 175 0 180	446 247 175 24 446	 +
Output Setup Total Setup Hold Removal Output Hold Total Hold Content Sugg Clock domain: mc - Input delay in STROBEn, mrst	243 242 0 24 266 +	23 0 0 0 +	180 5 175 0 180	446 247 175 24 446	 +



SmartTime Combinatorial Loops Report

Smart	lime [fii	nd_min]	- [Min	iimum D	elay A	na	lysis View]
<u> F</u> ile E	dit View	Actions	Tools	Window	Help		
			Cor Cor Timi Cor	nstraints Ei Instraint Wi Ing Analyz Instraint Ch	ditor zard er ecker	•	<u></u>
			Rep	orts		Þ	Report Paths
			Opt	ions			Report Violations Report Datasheet
ort							Report Bottlenecks Report Constraints Coverage Report Combinational Loops

- Combinatorial Loop Report
 - Displays all loops found during initialization
 - Reports pins associated with the loop(s), location where the loop is broken for timing analysis



Combinatorial Loop Report

🕺 jab - Combinational_loops Report		×			
File Actions Help					
βmartTime Version 3.0 Actel Corporation - Actel Desig	gner Software Release 8.4 (Version 8.4.0.0)	_			
Design Family Die Package Temperature Voltage Speed Grade Design State Analysis Min Case Analysis Max Case Scenario for Timing Analysis Using Enhanced Min Delay Analy	jab Fusion AFS600 484 FBGA COM -2 Post-Layout BEST WORST Primary				
<pre>& combinational loop has been of F_tns/tnsdelay0_sclr_0[1]:Y, F_tns/tnsdelay1/Qaux[6]:Q, I F_tns/tnsdelay0_sclr_0_a2[1] It has been broken between pins F_tns/tnsdelay0_sclr_0[1]:Y</pre>	detected between pins: , F_tns/tnsdelay1/Qaux[6]:CLR, F_tns/tnsdelay0_sclr_0_a2[1]:B, :Y, F_tns/tnsdelay0_sclr_0[1]:B and F_tns/tnsdelay1/Qaux[6]:CLR				
<pre>A combinational loop has been detected between pins: F_tns/tnsdelay0_sclr_0[0]:Y, F_tns/tnsdelay0/Qaux[6]:CLR, F_tns/tnsdelay0/Qaux[6]:Q, F_tns/tnsdelay0_sclr_0_a2[0]:B, F_tns/tnsdelay0_sclr_0_a2[0]:Y, F_tns/tnsdelay0_sclr_0[0]:B</pre>					
It has been broken between pins F_tns/tnsdelay0_sclr_0[0]:Y	and F_tns/tnsdelay0/Qaux[6]:CLR				
You may use the set_disable_tin which the loop is broken within	ming constraint to manually change the location of h a cell.				
		Σ			







Exporting SDF File

Extract Timing delays for post-layout simulation





- Steps
 - Route design
 - Export .sdf file (Back-annotate)
 - Run Post-layout Simulation
- SDF File Contains Delays for Min, Typ and Max





Click "Simulation" in Project Flow Window or...



Actel Corporation Confidential © 2009

486

- Structural Netlist and .sdf File Used for Simulation
 - Simulator runs for 1 uS as Default
 - Max Operating Conditions Default







Post-Layout Simulation Selecting Operating Conditions

Post-layout Operating Conditions

- Can Be Specified within Libero
 - Tools > Options from Libero Main Window
 - Select Simulation Tab in Options Window
 - Choose Min/Typ/Max

Project Settings			X
Device Flow Simulation			
ModelSim options	Name	Value	
Vsim command	SDF Timing Delays	О Min О Тур • Max	
Axcelerator	Resolution	1ps	
	Vsim additional options		
		Default	
	ОК	Cancel Help	



SmartPower

SmartPower Overview

- SmartPower Supports Axcelerator, RTAX-S, Fusion, IGLOO, ProASIC3, ProASIC^{PLUS} and ProASIC
- SmartPower Features:
 - Power Estimate for Individual Components in Design
 - Hierarchical Reports of Dynamic Power Consumption
 - Linked to SmartTime
 - Uses Clock Constraints
 - Support for Simulation Files:
 - VCD (Value-Change Dump)
 - SAIF (Synopsys Switching Activity Interchange Format)



SmartPower Overview





SmartPower Operating Conditions (1)

- Operating Conditions are Temperature, Voltage, Process
- Impact of Temperature:
 - High on Static Power,
 - Limited on Dynamic Power
- Impact of Process:
 - High on Static Power,
 - Limited on Dynamic Power
- Impact of Voltage:
 - High on Static Power,
 - High on Dynamic Power
- Impact of Radiation:
 - For RTAX-S, the TID reports show a very small rise in ICC at 100Krad. This rise in ICC is so small that it is in the range of error for experimental measurement, and therefore is insignificant
 - For RT-A3P, the TID reports show that this is also true for TID <
 40Krad



SmartPower Operating Conditions (2)

- Reminder about Best and Worst Corners Power
 - Power Corner definition differs from Timing
 - Best Power Corner:
 - Low Temperature, Low Voltage
 - Worst Power Corner:
 - High Temperature, High Voltage
 - For ProAsic3 COM for example
 - Best Power Corner: Temp= 0c, VCCA=1.425 V, VCCI = 3.0V
 - Typical Power Corner: Temp=25c, VCCA=1.5 V, VCCI = 3.3V
 - Worst Power Corner: Temp=70c, VCCA=1.575 V, VCCI = 3.6V



SmartPower Signal Activities

SmartPower Switching Activity Estimation is Based on the Concept of Clock Domains



- From Simple Model
 - Automatic Partitioning in Clock Domains by SmartPower
 - Only a few frequencies to set per Clock Domain
- To Accurate Model
 - Manual Partitioning
 - Pin by Pin annotation or Import Simulation file



Simulation Based Flow (1)

- Open Libero Simulation Options
- Check the "Generate VCD file" Checkbox Under "Do File"
- VCD File is Created Automatically During Simulation
 - Actel recommends performing postlayout simulation using the backannotated netlist when generating the VCD files





Simulation Based Flow (2)

- Simulation based estimation, User may still affect results
 - Quality of Simulation Trace
 - Post-Layout simulation versus RTL level simulation
 - Simulation for design coverage versus simulation to emulate true patterns and timings relationships, etc
 - Impact of glitches
- How do you know if your simulation is OK for power analysis?



SmartPower GUI

SmartPower GUI





SmartPower Summary Tab





SmartPower Summary Tab

Power Breakdown

- Display Power Consumption by Type, Rail or Clock Domain
 - Pie chart or grid display
- Type:
 - Displays a Breakdown of the Design's Power Usage by:
 - Net
 - Gate
 - I/O
 - Memory
 - Clock
 - Core Static
 - Banks Static
- Rail:
 - Displays a Breakdown of the Power Usage by Voltage rail
 - Power, Voltage, and Current Drawn are Displayed for each rail
- Clock Domain

1 SOC_TOP - SmartPower	
<u>File E</u> dit <u>V</u> iew <u>T</u> ools <u>S</u> imulation <u>H</u> elp	
🗟 🚹 🍓 🛢 🖣 🖣 🎒 🚳 🕅 Tyr	ical 🔻 MHz 🔻 mW 💌
Summary Comains Al Analysis	Activity Enable Rates
Power Consumption	
Total 61.7	02 mW
Static 24.9	5 mW
Dynamic 36.7	52 m₩
Breakdown By Type	Show 💌 Chart 🔿 Grid
By Type By Rail Power	Usage
By Clock Domain	
Core Static	11.839 mVV
7.5 mVV	Gate
Memory	1.969 mVV
15.305 m/V	
	Analog
3.798 mW	20.302 mVV
Operating Conditions : Typical	
Operating Conditions	Value
1 U Junction Temperature	25C
3 VCC33A	3.3 V
4 VCCI 3.3	3.3 V
Change Operating Conditions	
D-there	
Battery	
Battery capacity 1000.00 mA*H	rs Set
Battery life 31.138 Hour(s)	
	Active 25.00 C 1.50 V Speed: -2



SmartPower Summary Tab Power Breakdown – Grid View

Edil 1	t View Iools Simulation Help	ical 💽 MHz	▼ Wm ▼
5 Su	mmary 🛍 Domains 🗍 🔎 Analysis 🗍 🌊) Activity 🔰 🔒 Enable	Rates
Pow	er Consumption		
	Total 61.70	D2 mW	
	Static 24.95	5 mW	
	Dynamic 36.75	52 mW	
_			
Brea	kdown By Type	Show	C Chart C Grid
	Туре	Power (m₩)	Percentage
1	Net	11.839	19.2%
2	Gate	1.969	3.2%
3	Analog	20.302	32.9%
4	1/0	3.798	6.2%
5	Memory	15.305	24.8%
6	Core Static	7.500	12.2%
7	Banks Static	0.990	1.6%
Oner	ating Conditions : Tunical		
	Operating Conditions	Va	hue
1	Junction Temperature	25 C	
2	VCCA	1.5	5V
3	VCC33A	3.3 V	
4	VCCI 3.3	3.3	3V
<u>Cha</u>	ange Operating Conditions		
Batte	ary		
Ba	ttery capacity 1000.00 mA*H	rs Set	
	Nov. Ko. 21 120 U.S. (s)		



SmartPower Summary Tab Power Breakdown by Power Rail

Displays Power Consumption of all Power Rails

SOC_TOP - SmartPower	
<u>File E</u> dit <u>V</u> iew <u>T</u> ools <u>S</u> imulation <u>H</u> elp	
🐻 🚯 👌 🕞 🕞 🖓 Tyr	ical 🔻 MHz 💌 mW 💌
Summary 😡 Domains 🖓 Analysis 🕼	7 Activity Enable Rates
Power Consumption	
Total 61.7	D2 mW
Static 24.9	5 mW
Dynamic 36.7	52 mW
Breakdown By Rail	Show (Chart C Grid
Power Usage	Current Usage
	VCCI 3.3
4.788 mVV	1.451 mA
	6.066 mA
20.018 mW	
4 VCCA 36.897 mVV	
	VCCA 24,598 mA
De sestine Canditiana y Turical	
Operating Conditions : Typical	
Uperating Conditions	Value 25.0
2 VCCA	1.5V
3 VCC33A	3.3 V
4 VCCI 3.3	3.3 V
Change Operating Conditions	
Battery	
	12 261
Battery life 31.138 Hour(s)	
Ready	Active 25.00 C 1.50 V Speed: -2

SOC_TOP - SmartPower			
<u>File Edit View T</u> ools Simulation <u>H</u> elp			
💿 🚹 🦓 📮 🖣 🗗 🎒 🔞	Typical	▼ MHz	▼ mW ▼
😢 Summary 🔯 Domains 🛛 🔊 Analysis	R Activity	By Enable Rate	s]
- Power Consumption			
Total	61.702 mW		
Static	24.95 mW		
Dynamic	36.752 mW		
Breakdown - By Rail		— Show C (Chart 💿 Grid
Rail Name	Power (m₩)	Voltage (V)	Current (mA)
1 VCCA	36.897	1.500	24.598
2 VCC33A	20.018	3.300	6.066
3 VCCI 3.3	Rail Name Power (mW) Voltage (V) Current (mA) 36.897 1.500 24.598 A 20.018 3.300 6.066 .3 4.788 3.300 1.451		
Operating Conditions : Typical			
Operating Conditions		Value	
1 1 Junction Temperature		25 C	
2 VCCA		1.5 V	
3 VCC33A		3.3 V	
4 VCU 3.3		3.3 V	
Change Operating Conditions			
Battery			
Battery capacity 1000.00	mA*Hrs Set		
Battery life 31.138 Hour(s)			
l Readu		Active 25	00 C 1 50 V Speed: -2
itoday		Heave 23.	



SmartPower Summary Tab Power Breakdown by Clock Domain

Displays Power Consumption of all Clock Domains

* SOC_TOP - SmartPower	
<u>File Edit View Tools Simulation H</u> elp	
💿 🚯 🖓 📮 🗣 🛍 🎒 🔞 😶 Тур	ical 💌 MHz 💌 mW 💌
🍋 Summary 🛍 Domains 🖾 Analysis 🕅	Activity Enable Rates
Power Consumption	
Total 61.70	12 mW
Static 24.95	j mW
Dynamic 36.75	j2 mW
Breakdown By Clock Domain	Show 👁 Chart 🔿 Grid
Power	Usage
Other Domains	
	5.12 mW
9.494 mW	
	20.896 mW
Operating Conditions : Typical	
Operating Conditions	Value
2 VCCA	
3 VCC33A	3.3 V
4 VCCI 3.3	3.3 V
Change Operating Conditions	
Battery	
Battery capacity 1000.00 mA*H	s Set
Battery life 31.138 Hour(s)	
l	
кеаду	Active [25.00 C [1.50 V [Speed: -2]

0	⊻iew <u>T</u> ools 3 B G	Simulation He	lp W Typic	cal 💌 MHz	▼ mW	•
5 Summ	iary 📷 D	omains 🗌 🔎 Anal	lysis 🛛 😰	Activity 🕴 🔒 Enable	Rates	
Power C	Consumption					
		Total	61.702	2 mW		
		Static	24.95	m₩		
		Dynamic	36.75	2 mW		
Breakdo	wn By C	lock Domain 🗖	-	Show	C Chart 💽 Grie	ġ
		Domain		Power (mW)	Percentage	^
1 B/	COSC100M	0/RCOSC1:CLKC	JUT (Clock)	5.120	13.9%	
2 R	COSC100M	0/RCOSC1:CLKC)UT (Data)	0.000	0.0%	
3 C8	8051BASIC_	0/COREAI_0/CO	REAI_oloi[1	0.026	0.1%	
4 C8	8051BASIC	_0/COREAI_0/CO	REAI_oloi[1	0.423	1.1%	
5 C8	8051BASIC	_0/U_8051s_0/U_	8051s_0/C	0.572	1.6%	
5 C	SUSTBASIC	_U/U_8051s_U/U_ `CLA (Clask)	8051s_0/C	0.221	0.5%	-
2 CI	LKGEN_0/C	ore:GLA (Clock)		20.036	25.3%	
		,orc.albh (b'd(d)		0.000	0.00	
Operatin	ng Condition:	s : Typical —				
Operatin	ng Condition: Ope r	s : Typical ating Condition	S	Val	ue	
Operatin	ng Condition: Ope r Ju	s: Typical ra ting Condition nction Temperatur	e	Val 25	ue C	
Operatin	ng Condition: Ope r Ju	s: Typical rating Condition nction Temperatur VCCA	e	Val 25 1.5	lue C V	
Operatin 2 3	ng Conditions Oper Ju	s: Typical rating Condition nction Temperatur VCCA VCC33A VCC13.2	8 6	Val 25 1.5 3.3	lue C SV SV	
Operatin 2 3 4	ng Condition: Oper Ju	s: Typical rating Condition nction Temperatur VCCA VCC33A VCC33A VCC1 3.3	1 S	Val 25 1.5 3.3 3.3	lue C SV SV SV SV	
Operatin 1 0 2 3 4 Change	ng Condition: Oper 'Ju	s : Typical rating Condition nction Temperatur VCCA VCC33A VCCI 3.3 Conditions	8 6 	Val 25 1.5 3.3 3.3 3.3	lue C SV SV SV	
Operatin 1 0 2 3 4 Change Battery-	ng Conditions Oper Ju e Operating	s : Typical	1 5	Val 25 1.5 3.3 3.3	lue C SV SV SV	
Operatin 1 0 2 3 4 Change Battery- Battery	e Operating	s : Typical rating Condition nction Temperatur VCC33A VCC1 3.3 Conditions	ns e mA*Hrs	Va 25 1.5 3.3 3.3 3.3 8 8	lue C SV SV SV	
Operatin 1 0 2 3 4 Change Battery Battery Battery	ng Conditions Oper Ju e <u>Operating</u> y capacity y life	s : Typical rating Condition nction Temperatur VCC33A VCCI 3.3 Conditions 1000.00 31.138 Hour	1 5 e mA*Hrs	Va 25 1.5 3.3 3.3 8 9 5 Set	lue C SV 3V 3V	


SmartPower Summary Tab

Junction Temperature

- SmartPower Estimates Junction Temperature (T_J)
- Junction Temperature can be Calculated from Operating Conditions or Ambient Temperature
 - $T_{J} = T_{A} + \theta_{JA} * (P_{dynamic} + P_{static})$ $\theta_{JA} (Package Thermal Resistance)$
- Cooling Scenarios:
 - Still Air (default)
 - 300 ft / min
 - Case Cooling
 - Custom
- SmartPower Reports the Thermal Resistance θ_{JA}

SOC_TOP - SmartPower	
<u>File E</u> dit <u>V</u> iew <u>T</u> ools <u>S</u> imulation <u>H</u> elp	
💿 🚯 🖓 📮 🖏 🟝 🎒 🔞 🛺 Typ	ical 💌 MHz 💌 mW 💌
	ana lever l
Summary (Intro Domains) All Analysis (Intro	Activity BRE Enable Rates
Power Consumption	
Total 61.70	02 mW
Static 24.95	5 mW
Dynamic 36.75	52 m₩
Breakdown By Type	Show 💿 Chart 🔿 Grid
Power	Usage
Banks Static 0.99 mW Core Static 7.5 mW Memory 15.305 mW 3.798 mW	Net 11.839 mVV Gate 1.969 mVV Analog 20.302 mVV
Uperating Conditions : Typical	
Operating Conditions	Value
2 VCCA	
3 VCC33A	3.3V
4 VCCI 3.3	3.3 V
Change Operating Conditions	
Battery	
Battery capacity 1000.00 mA*H	rs Set
Battery life 31.138 Hour(s)	
ı Ready	Active 25.00 C 1.50 V Speed: -2



SmartPower Domain Tab (1)

- Actel Vector-less Approach
 - Clock Constraints extracted form SmartTime
 - A distinct toggle rate can be set per clock domain & per type of net

Summary Context Context	
Status Name (MHz) outputs (MHz) (MHz) output V CortexM1_00/CortexM1Top_ 50 3 (12 %) 0 (0 %) 3 (12 %) 5.75 (national
CortexM1_00/CortexM1Top_ 50 3 (12 %) 0 (0 %) 3 (12 %) 5.75 (ts (MHz)
	(23 %)
CortexM1_00/CortexM1Top_ 10 1 (20 %) 0 (0 %) 0.05 (1 %) 0.05	(1%)
SYSCLK 25 1.875 (15 %) 0 (0 %) 2.875 (23 %) 3 (2	24 %)
V ujtag_UJTAG_TCK 25 0.287 (2.3 %) 0 (0 %) 0.312 (2.5 %) 1.25 ((10 %)

If you don't have simulation data, this step is crucial for the quality of the estimation. Beware that Garbage-In => Garbage-Out



SmartPower Domain Tab (2)

- Garbage-In => Garbage-Out.... What Do We mean?
 - Default Vector-less flow: Clock Constraints are taken from SmartTime

1 <mark>0</mark> m	1_igloo_pro	oc * - SmartPower					
File	Edit View T	ools Simulation Help					
6	🔒 🚳 📄	📑 🖻 🎒 🔯 💮 🛛 Ty	pical 🗾 MH2	z 🔻 mW	-		
	Summary	Domains Analysis	equencies Rt Probal	bilites			
SI SI	how: •	Frequencies C Probabilities					
_ Cle	ock domains –						
	Status	Name	Clocks (MHz)	Register outputs	Set/Reset nets (MHz)	Primary inputs (MHz)	Combinational outputs (MHz)
1	 	CortexM1_00/CortexM1Top_	50	2.5 (10 %)	0(0%)	2.5 (10 %)	2.5 (10 %)
2	Δ	CortexM1_00/CortexM1Top_	0	0(0%)	0(0%)	0 (0 %)	0 (0 %)
3	_	SYSCLK	25	1.25 (10 %)	0 (0 %)	1.25 (10 %)	1.25 (10 %)
4		ujtag_UJTAG_TCK	25	1.25 (10 %)	0(0%)	1.25 (10 %)	1.25 (10 %)
		Alv	vays veri have a	fy that y correct	your clock value!	S	
							Hide act of pins
_ Se	et of pins ——						The set of pins
	Status			Name			Data (MHz)
	V 1	lusenableSet					U
Fre	quencies and I notation).Chang	Probabilities displayed in this tab are c ging these values may not impact pow	lefault values. They are ver estimation, dependi	used for nets that h ng on the percentag	nave not been annotated ge of nets annotated.	by any method (i.e. VCD o	or manual
Ready						Active	25.00 C 1.50 V Speed: STD



SmartPower Domain Tab (3)

- Garbage-In => Garbage-Out.... What Do We mean?
 - Default Vector-less flow: All Toggle Rates are set to 10%

1 0 n	n1_igloo_pro	oc * - SmartP	ower						
File	Edit View T	ools Simulation	Help						
8	🔒 🗟	🖣 🖣 🎒	🔯 🐵 🛛 Ts	ypical 💽 MH;	z 💌 mW	•			
e e	Summary	Domains	Analysis 🛛 🐼 Fn	equencies 🛛 🔒 Probal	bilites	100 % То F _{DATA} = F	ggle Rate	means	-
l _E C	lock domains –				L	DAIA	CLOCK		
IΓ	Status	N	ame	Clocks (MHz)	Register outputs	Set/Reset nets (MHz)	Primary inputs (MHz)	Combinational outputs (MHz)	-
1		CortexM1_00)/CortexM1Top_	50	2.5 (10 %)	0(0%)	2.5 (10 %)	2.5 (10 %)	
2	. 🗸	CortexM1_00)/CortexM1Top_	25	1.25 (10 %)	0 (0 %)	1.25 (10 %)	1.25 (10 %)	
3		SYSCLK		25	1.25 (10 %)	0 (0 %)	1.25 (10 %)	1.25 (10 %)	
4	· · · ·	ujtag_UJTAG	_тск	0	0(0%)	0(0%)	1.25 (0 %)	1.25 (0 %)	
	10% except Set/Reset nets. Is 10% appropriate for your design?								
S	et of pins							<u>Hide set of pi</u>	<u>ins</u>
	Status	(OsEnableSet			Name			Data (MHz)	
Fr	equencies and F notation).Chang	Probabilities displa ging these values	ayed in this tab are o may not impact pov	default values.They are ver estimation, dependi	used for nets that h ng on the percentag	nave not been annotated ge of nets annotated.	by any method (i.e. VCD)	or manual	
Read	y						Active	25.00 C 1.50 V Speed: 5	STD /



SmartPower Domain Tab (4)

 Default vector-less flow with 10% toggle rates leads to +/- 100% error when compared to a simulation flow





SmartPower Domain Tab (5)

Improved Vector-less flow: Design specific Toggle Rates

*]] m1_igloo_proc * - SmartP	ower						
File Edit View Tools Simulation	Help						
6 6 8 8 8 8 8	🗟 😡 🛛 Tv	pical 🔽 MHz	▼ mW ▼				
Modes and scenarios		·····	<u> </u>				
Pre-defined modes	🛛 💼 Summary 🛛 🖻	🗑 Domains 🛛 🗯 Analysis 👘	Requencies	Probabilites			
Active							
Flash*Freeze							
Sleep	snow: 💌	Frequencies O Probab	olities				
Static	Clock domains -						
Pre-defined scenarios			Clocks	Register	Set/Reset nets	Primary inputs	Combinational
50% Flash*Freeze	Status	Name	(MHz)	outputs	(MHz)	(MHz)	outputs (MHz)
80% Flash*Freeze	1 🗸	CortexM1_00/Cortex	50	5 (20 %)	0(0%)	3 (12 %)	4.25 (17 %)
95% Flash"Freeze	2	CortexM1_00/Cortex	25	1.875 (15 %)	0(0%)	1.25 (10 %)	1.5 (12 %)
	3 🗸	SYSCLK	25	0.625 (5 %)	0 (0 %)	0.625 (5 %)	0.875 (7 %)
	4 🗸	ujtag_UJTAG_TCK	0	0(0%)	0(0%)	1.25 (0 %)	1.25 (0 %)
		User set	s a diffe clock ar	erent to nd per	ggle-rate type of n	e value et	
	Set of pins						Hide set of pins
	Status			Name			(MHz)
	1 🖌 🛛	IOsEnableSet					0
New custom mode New custom scenario All simulation files are processed	Frequencies and annotation).Chance	Probabilities displayed in this aina these values may not im	tab are default values pact power estimation	They are used for depending on the	nets that have not been percentage of nets ann	annotated by any metho otated.	od (i.e. VCD or manual
Ready						Active 25.0	00 C 1.50 V Speed: STD //



SmartPower Domains Tab Initialize Frequencies

Tools > Initialize Frequencies and Probabilities

Ele Edit View Tools Simulation Help Image: Summary Domains Analysis Image: Summary Domains Image: Summary Domain	1 SOC_TOP - SmartPower				
Clock Name Clock Freq. MHz Data Freq. MHz I InputSet 0 2 0 RCOSCIOM_0/RCOSC1:CL 100 3 C8051BASIC_0/COREAI_0/C 10 0.5 (10 %) 4 C8051BASIC_0/COREAI_0/C 10 0.5 (10 %) 5 0 CLKGEN_0 Select a Category: Clocks 6 TCK Select a Category: Clocks 9 Preaker helds Others Select a Category: Clocks 0 Tetales clock frequencies and dxy cycles Select a Category: Clocks 9 Select a Category: Clocks Select a Category: Select a Category: 0 DP Register outputs Select a Category: Select a Category: Select a Category: Select a Category: 0 Others Use SmartTime With ded constraint if available in SmartIme Select a Category: Select a Category: <td< th=""><th>File Edit Yiew Tools Simulatio</th><th>on <u>H</u>elp 🖌 i 🔀 💮 Typical 💽 [t</th><th>MHz 💌 mW 💌</th><th></th><th></th></td<>	File Edit Yiew Tools Simulatio	on <u>H</u> elp 🖌 i 🔀 💮 Typical 💽 [t	MHz 💌 mW 💌		
Clock Status Name Clock Freq. MHz Data Freq. MHz 1 InputSet 0 2 RCOSCI00M_0/RCOSCI:CL 100 5 (10 %) 3 C8051BASIC_0/COREAI_0/C 10 0.5 (10 %) 4 C8051BASIC_0/COREAI_0/C 10 0.5 (10 %) 5 CLKGEN_0 SmartPower - Initialize Frequencies and Probabilities X 6 TCK Select a Category: Clocks 1 Clocks Primary inputs Constant if available in SmartTime Clock Constraints Select a Category: Incode 90.00 % Selfers outputs With clock constraint if available in SmartTime USee SmartTime Select outputs With clock constraint if available in SmartTime 0 Clock Constraints Specify default frequency 10.00	🗞 Summary 🛍 Domains 💡	🕰 Analysis 🛛 🗞 Activity 🔹 🕏 Er	nable Rates		
Clock Status Name Clock Freq. MHz Data Freq. MHz 1 InputSet 0 2 3 RCOSC100M_0/RCOSC1:CL 100 5 (10 %) 3 A C8051BASIC_0/COREAL_0/C 10 0.5 (10 %) 4 C8051BAS SmartPower - Initialize Frequencies and Probabilities Image: Clock Second Seco				Create Domain	
1 InputSet 0 2 0 RCOSC100M_0/RCOSC1:CL 100 5 (10 %) 3 A C8051BASIC_0/COREAI_0/C 10 0.5 (10 %) 4 C8051BAS SmartPower - Initialize Frequencies and Probabilities Image: Constraint of the second s	Clock Status	Name	Clock Freq. MHz	Data Freq. MHz	
4 C8051BAS SmartPower - Initialize Frequencies and Probabilities Image: Clock Sector a Category: Image: Clock Sectory: Image: Clock Sector a Category: <th></th> <th>InputSet RCOSC100M_0/RCOSC1:CL C8051BASIC_0/COREAI_0/C</th> <th>100 10</th> <th>0 5 (10 %) 0.5 (10 %)</th> <th></th>		InputSet RCOSC100M_0/RCOSC1:CL C8051BASIC_0/COREAI_0/C	100 10	0 5 (10 %) 0.5 (10 %)	
General Clocks Set/Reset nets Set/Reset nets Primary inputs Combinational outputs Set of pins Use SmartTime Clock Constraints Specify default frequency Specify default frequency		C8051BAS SmartPower - Initialize I CLKGEN_0 TCK Select a Category:	Frequencies and Probabilities Clocks		
		General Clocks Set/Reset nets Set/Reset nets Set/Reset nets Combinational outputs Set of pins Enables Others Use Smarr Clock Cons Specify c	tTime traints default frequency	requencies and duty cycles onstraint if available in SmartTime efault frequency 10.00 MHz and duty cycle 50.00 %	

"Initialize Frequencies" Button



SmartPower Analysis Tab

 Provides Hierarchical Report of Dynamic Power Consumption



SmartPower Analysis Tab Power Breakdown By Type

- Analysis Grid Displays Power Breakdown for Selected Block by:
 - Net, Gate, I/O, Memory, Clock, Core Static, Banks Static
 - Grid or pie chart display



SmartPower Analysis Tab Power Breakdown By Instance

 Analysis Grid Displays Power of all Sub-elements of Selected Block

	SOC_TOP - SmartPower							
	File Edit View Tools Simulation Help			_		[]		
		9	Typical MH:	z <u> </u>	m\\ _			
	😢 Summary 🛛 🛍 Domains 🖉 Analy	ysis	Activity Retrable	e Rates]			
		Br	Power Consumption Block Name: S Static Power: 2 Dynamic Power: 3 reakdown: By Instance Instances Contributions ▼ Blocks ▼ Nets	50C_T0 24.95 mV 36.752 m	P V W J Gates V	I/Os 🔽 Memor	ies	Apply
	RCDSC100M_0	[Name	Туре	 Power (mW) 	Driver	Fanout	Macro
	Flash4Kx8_wrapper_0	1	C8051BASIC_0	Block	23.013			C8051BASIC
Limit components to be	🚺 🔤 🖬 Flash4Kx8_wrapper_0/F	2	Data_RAM4Kx8_	Block	6.5			Data_RAM4Kx8_
Limit components to be	🔤 👪 Shift7_0	3	Pgm_RAM4Kx8_	Block	6.5			Data_RAM4Kx8
dignlound by checking on		4	CLKGEN_0_GLA	Net	5.995	CLKGEN_0/Core	485	
displayed by checking or		5	RCOSC100M_0	Block	4.95			RCOSC100M
un checking boxed		6	Flash4Kx8_wrap	BIOCK	1.534			
un-checking Doxes	•		uataout_pad[0]	1/0	0.475			
	Ready	, 1				Ac	tive 25.0	D C 1.50 V Speed: -2



SmartPower Activity Tab

- Allows Entry of Switching Activity Information on Interconnects of Design
 - Use to Confirm Data Entered through VCD or SAIF File Import or pin-by-pin annotation

Driver: * Set Domain: All Source: All Driver Net Domain Free 1 TDI 2 TMS 3 TRSTN 4 ATRETURN4 Source: All Source: A	uency Source Default
DriverNetDomainFree Pree <th>1Hz Source Default</th>	1Hz Source Default
TDI TDI InputSet 0 TMS TMS TMS 0 TRSTN TRSTN InputSet 0 ATRETURN4 ATRETURN4 InputSet 0	Default
2 TMS TMS InputSet 0 3 TRSTN TRSTN InputSet 0 4 ATRETURN4 ATRETURN4 InputSet 0	
3 TRSTN TRSTN InputSet 0 4 ATRETURN4 ATRETURN4 InputSet 0	Default
4 ATRETURN4 ATRETURN4 InputSet 0	Default
	Default
5 C8051BASIC_0/COREAI_0/COREAI_1010 C8051BASIC_0/COREAI_0/COREAI_LL1 InputSet 0	Default
6 AT9 AT9 InputSet 0	Default
7 C8051BASIC_0/COREAI_0/COREAI_li00_C8051BASIC_0/COREAI_0/COREAI_ol1[InputSet 0	Default
8 AV0 AV0 InputSet 0	Default
9 C8051BASIC_0/COREAI_0/COREAI_00_C8051BASIC_0/COREAI_0/COREAI_00[InputSet 0	Default
10 SYS RESET SYS RESET InnuitSet 0	Default
Annotate selected pins	Select a





SmartPower Enable Rates Tab

- Specify Output Enable Rate for Each Bi-directional and Tristate I/O
 - Percentage of Time I/O is used as an Output

* SOC_TOP - SmartPower				
<u>File E</u> dit <u>V</u> iew <u>T</u> ools <u>S</u> imulation <u>H</u> elp				
💿 🚹 🖓 🖹 📲 🗈 🎒 🔯 💮 Typical	▼ MHz ▼ mW ▼			
📚 Summary 🛛 📾 Domains 🗍 🔎 Analysis 🔹 🚱 Activity	₿¢ Enable Rates			
Driver: * Set Type: All	▼ Polarity: All ▼ Source: A	•		
Driver	Net	Type Polar	ity Rate %	Source
1 AND2_0:Y	AND2_0_Y	Memories Low	12.5	Default E
2 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8	Data_RAM4K×8_0_WEAP	Memories Low	12.5	Default E
3 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8	Pgm_RAM4Kx8_0_WEAP	Memories High	12.5	Default E
4 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8	C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8	Memories Low	12.5	Default E
5 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8	C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8	Memories High	12.5	Default E
	Specify Enable ro individual I/O pin	ites for s		
Ready		آ اً	Active 25.00 C	▼ 1.50 V Speed: -2



SmartPower Importing a VCD or SAIF File

 Switching information for the design can be entered by importing a VCD or SAIF file

1 SOC_TOP - SmartPower	
File Edit View Tools Simulation Help	
🐻 🚹 👌 📑 Import VCD File iical 💌 MHz 💌	mW 💌
Remove VCD File > 7 Activity Charles	
Audit files	
Driver: Set Type: All 💌 Polar	rity: All 💌 Source: All 💌
Driver	t VCD Options
1 AND2_0:Y AND2_0. 2 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8 Data_RA 3 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8 Data_RA	ect a Category: General
3 C8051BASIC_0/0_8051s_0/0_8051s_0/CORE8 Pgm_RA VCD p 4 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8 C8051BA Pa 5 C8051BASIC_0/U_8051s_0/U_8051s_0/CORE8 C8051BA To	parsing options artial parsing polevel name
	litch filtering VCD file:
	Import in:
	Existing mode: Active ✓
	O New mode:
Import VCD Eile	Help OK Cancel



Simulation File Import Options

Specify start and end times for partial parsing of simulation file

Import VCD Options		
Select a Category: General VCD parsing options Partial parsing Top level name Glitch filtering	Partial parsing Partially parse VCD Start time: End time:	0.00 ns 10000.00 ns
Help		OK Cancel

Specify glitch filtering •Automatic or user-defined threshold





Actel Corporation Confidential © 2009

Simulation Based Flow

Verify Simulation Coverage and Frequencies

Driver:	ng Frequencies:	Set Domain:	cik 💽 Source: All				
	Driver	Net	Domain	Frequency (MHz)	Source		
1 2 3 4 5 6 7 8 9 10 11 11	UUT/u2/inf_2_0_ UUT/u2/inf_2_0_ UUT/u2/inf_2_0: UUT/u6/II_0/U1/i UUT/u6/II_0/U1/i UUT/ifdiv_opa_w clk UUT/ifdiv_opa_w UUT/ifdiv_opa_w UUT/u6/II_0/U1/ UUT/u6/II_0/U1/	UUT/u2/inf_2_0_ UUT/u2/inf_2_0_ UUT/u2/inf_2 UUT/u6/II_0/U1/ UUT/u6/II_0/U1/ UUT/u6/II_0/U1/ UUT/div_opa_w[UUT/d6/II_0/U1/ UUT/u6/II_0/U1/ UUT/u6/II_0/U1/ UUT/u6/II_0/U1/	clk (combinational outputs) clk (combinational outputs) clk (combinational outputs) clk (register outputs) clk (register outputs) clk (register outputs) clk (combinational outputs)	0.593853 0.148765 0.142566 0.537378 0 0 0.449566 3.4481 0 0 0	VCD Import VCD Import VCD Import VCD Import VCD Import VCD Import VCD Import VCD Import VCD Import	t all	
-Average Clock: Regist Set/Re Primar	e Frequencies: 3.448 teroutputs: 0.115 eset nets: 0 y inputs: 0 primuts: 0	MHz MHz MHz MHz 0.029 MHz	Annotation Stal VCD Import: Manual Annot Default Estima	istics: stion: tion:	100 % 0 % 0 %		

You can also check your Frequencies by type of element: clocks, inputs, set/reset...

If VCD import < 95%, I would suspect wrong VCD or behavioral VCD



Simulation Based Flow Cycle Accurate Power Analysis

 Use Cycle Accurate Analysis to "debug" your Simulation in Terms of Power



Power Analysis

Power Consumption For Specific Clock Domain

- Confirm SmartPower is in Toggle-rate Mode (Default Setting)
 - Confirm "Use Toggle Rates" Option is Checked in SmartPower Preferences
- Set all the Clock Frequencies Except the Clock Domain of Interest to Zero in the Domains tab
 - The Total Power Consumption for Clock Domain is Displayed in the Summary tab
 - Includes the contribution of the clock buffer, clock tree, and all clock input of the registers of specific clock domain
- To Determine the Power of the Clock Tree Only, set the Toggle Rate of the Data for the Clock Domain to Zero
 - Total Power Displayed is the Power of the Clock Tree



Power Analysis Dynamic I/O Power – Analysis Tab

- Select the Highest Hierarchy Level in the Hierarchy tree in the left pane and Select "By Instance" from the Breakdown drop-down list
- Un-check all categories under Instances Contributions except I/Os
 - The table displays a list of all I/Os in the design and the power contribution of each individual I/O

1 1 4 1 4 4 6	Typical	<u>▼</u> MHz	- m	w 🔳						
🗞 Summary 🛛 🛍 Domains 🔎 Analysis	Co Acti	vity 🛛 🔒 Enable Rab	es							
	Pow	er Consumption								
Data RAM4Kx8 0		Block Name:	soc_то	P						
RAM_mux_0		Static Power	24.95 m\	N						
E C8051BASIC_0		Durani Duran	26 752 8	au						
E C8051BASIC_0/U_GPI0_0		Dynamic Power:	30.73211							
E C8051BASIC_U/CoreAPB	Sec. an									
	D 1			and the second sec						
□ ↓ C8051BASIC_0/U_8051s_0	Break	down: By Instance		_						
	Break	down: By Instance	-	_			1			
	Break	down: By Instance ances Contributions Blocks I Nets	Г	💌 Gates 🔽	1/Os 🗖 Memo	ries 🗌	Apply			
	Break	down: By Instance ances Contributions Blocks Nets	Г	Gates 🔽	I/Os ∏ Memo	ries [1/0	Qutrut	
	Break	down: By Instance ances Contributions Blocks T Nets Name	Г	Gates V Power (mW)	1/Os T Memo	ries	Apply Macro	I/O Standard	Output Load (pF)	
	Break	down: By Instance ances Contributions Bocks Nets Name C8051BASIC_0	Г Туре Block	Gates V Power (mW) 23.013	I/Os Memo Driver	ries Fanout 	Apply Macro C8051BASIC	I/O Standard 	Output Load (pF)	
	Break	down: By Instance ances Contributions Bocks T Nets Name C8051BASIC_0 Data_RAM4K×8_	Type Block Block	Gates ✓ Power (mW) 23.013 6.5	I/Os Memo Driver 	Fanout	Apply Macro C8051BASIC Data_RAM4Kx8_	I/O Standard 	Output Load (pF) 	
	Break	down: By Instance ances Contributions Bocks Nets Name C8051BASIC_0 Data_RAM4K×8_ Pgm_RAM4K×8_	Type Block Block Block	Cates Power (mW) 23.013 6.5 6.5	1/Os Memo Driver 	Fanout	Apply Macro C8051BASIC Data_RAM4Kx8_ Data_RAM4Kx8	I/O Standard 	Output Load (pF) 	
	Break	down: By Instance ances Contributions Blocks Nets Name C8051BASIC_0 Data_RAM4K×8_ Pgm_RAM4K×8_ CLKGEN_0_GLA	Type Block Block Block Net	▼ Gates ▼ Power (mW) 23.013 6.5 6.5 5.995	I/Os Memo Driver CLKGEN_0/Core	ries Fanout 485	Apply Macro C8051BASIC Data_RAM4Kx8_ Data_RAM4Kx8	I/0 Standard 	Output Load (pF) 	
	Break	down: By Instance ances Contributions Blocks Nets Name C8051BASIC_0 Data_RAM4Kx8_ Pgm_RAM4Kx8_ CLKGEN_0_GLA RCOSC100M_0	Type Block Block Block Net Block	▼ Gates ▼ Power (mW) 23.013 6.5 6.5 5.995 4.95	I/Os Memo Driver CLKGEN_0/Core 	ries	Apply Macro C8051BASIC Data_RAM4Kx8_ Data_RAM4Kx8 RCOSC100M	I/0 Standard 	Output Load (pF)	
	Break	down: By Instance ances Contributions Blocks Nets Name C8051BASIC_0 Data_RAM4K×8_ Pgm_RAM4K×8_ CLKGEN_0_GLA RCOSC100M_0 Flash4K×8_wrap	Type Block Block Block Net Block Block	▼ Gates ▼ Power (mW) 23.013 6.5 6.5 5.995 4.95 1.534	I/Os Memo Driver CLKGEN_0/Core 	Fanout 485 	Apply Macro C8051BASIC Data_RAM4Kx8_ Data_RAM4Kx8 RCOSC100M Flash4Kx8_wrap	I/0 Standard 	Output Load (pF) 	
	Break Insta I 1 2 3 4 5 6 7	down: By Instance ances Contributions Blocks Nets Name C8051BASIC_0 Data_RAM4K×8_ Pgm_RAM4K×8_ CLKGEN_0_GLA RCOSC100M_0 Flash4K×8_wrap dataOut_pad[0]	Type Block Block Block Block Net Block Block	▼ Power (mW) 23.013 6.5 6.5 5.995 4.95 1.534 0.475	I/Os Memo Driver CLKGEN_0/Core 	ries	Apply Macro C8051BASIC Data_RAM4Kx8_ Data_RAM4Kx8 RCOSC100M Flash4Kx8_wrap ADLIB:OUTBUF	I/0 Standard LVTTL	Output Load (pF) 35	
 ☐: C8051BASIC_0/U_8051s_0 ☐: C8051BASIC_0/U_8051s ☑: C8051BASIC_0/COREAL_0 ☑: CLKGEN_0 ☑: RAM_mux_1 ☑: RCOSC100M_0 ☐: Flash4Kx8_wrapper_0 ☑: Flash4Kx8_wrapper_0/FLAS ☑: Shift7_0 	Break	down: By Instance Inces Contributions Nocks Nets Name C8051BASIC_0 Data_RAM4Kx8_ Pgm_RAM4Kx8_ CLKGEN_0GLA RCOSC100M_0 Flash4Kx8_wrap dataOut_pad[0]	Type Block Block Block Block Net Block Block I/O	▼ Gates	I/Os Memo Driver CLKGEN_0/Core 	Fanout	Apply Macro C8051BASIC Data_RAM4Kx8_ Data_RAM4Kx8 RCOSC100M Flash4Kx8_wrap ADLIB:OUTBUF	I/0 Standard LVTTL	Output Load (pF) 35	



SmartPower Operating Conditions

SmartPower Junction Temperature Operating Conditions - General

Select Operating Conditions





SmartPower Junction Temperature Operating Conditions – Temperature Settings

- Define Temperature Settings:
 - Default, Custom Operating range or Mode by Mode range

SmartPower - Operating Condition	15	×
Select a Category: General Comperature settings Thermal resistance settings Voltage settings VOCA VCC33A VCCI 3.3	Temperature settings Use: Design operating range (default) Smart Design operating range (default) Custom operating range evice Selection Wizard: Mode by mode operating range mode by mode operating range Junction Temperature (in degrees Celsius) Dest: Typical: Worst: 0.00 25.00 70.00	
Help	OK Cancel	



SmartPower Junction Temperature Operating Conditions – Temperature Settings

- Define Temperature Settings:
 - Default, Custom Operating range or Mode by Mode range
 - Specify ambient or junction temperature in custom settings

SmartPower - Operating Condition	15	×
Select a Category: General Temperature settings Thermal resistance settings Voltage settings VOCA VCC33A VCCI 3.3	Temperature settings Use: Design operating range (default) Smart Design operating range Custom operating range evice Selection Wizard: Mode by mode operating range mode operating range Junction Temperature (in degrees Celsius) Eest: Typical: Worst: 0.00 25.00 70.00	
Help	OK Cancel	



SmartPower Custom Ambient Temp

Advanced: Custom Ambient Temperature Settings:

SmartPower - Operating Conditio	ns				
Select a Category: General Comperature settings Thermal resistance settings Voltage settings Voltage settings VCC VCCI 3.3	Temperature settings Use: Custom operating range SmartPower uses a custom operating range that can be specified bell This custom operating range applies to SmartPower only. Specify (in Celcius degrees): O Junction Temperature Ambient Temperature	w.	MHz	mW ImW Frequencies Immunol 08.136 mW 04.243 mW 886 mW Sho Sho	l≯ Probabilites] w C Chart I® Grid
	Best: Typical: Worst: 0.00 25.00 80.00		Туре	Power (mW) 2.300 0.498 1.089 101.751 2.498	Percentage 2.1% 0.5% 1.0% 94.1% 2.3%
Help	OK Cancel		we · Worst		
You can the Junc an ambient	ask SmartPower to compute tion Temperature based on Temperature that you specify	Battery	voice of the conditions which the conditions which the conditions which the conditions with the conditions	¥ 8 ▲ 82 1.5	alue 0 C 2.82 C 375 V 3 V
This compu automatica	ted Junction temperature is <u>not</u> ally propagated to SmartTime.	Battery capacity Battery life	1000.00 mA	A*Hrs Set	82.82 C 1.58 V Speed: -2



SmartPower Computes Junction Temp

Junction Temperature Computation:





SmartPower Junction Temperature Operating Conditions – Thermal Resistance Settings

- Define Cooling Scenarios
 - Pre-defined or custom

SmartPower - Operating Condition	ns	
Select a Category: General Comperature settings Thermal resistance settings Voltage settings VOCA VCC33A VCCI 3.3	Thermal resistance settings Select the thermal characteristic for $\widehat{\Theta}_{Tr}$ ● Pre-defined: Still Air 26.6 C/W ● Custom: 1.0 m/s 2.5 m/s Select the setting only applies if you specify Ambient temperature in the 'Temperature settings' page.	
Help	OK Cancel	



SmartPower Custom Voltage Settings

- Define Custom Voltage Settings
 - Operating range, custom operating range or mode by mode

SmartPower - Operating Condition	ns	×
Select a Category: General Comperature settings Thermal resistance settings Voltage settings Voltage settings VCCA VCC33A VCCI 3.3	VCCA Use: Design operating range (default) Smart Design operating range (default) Custom operating range wice Selection Wizard: Mode by mode operating range wice Selection Wizard: Voltage (in volts) voltage (in volts) Best: Typical: Worst: 1.425 1.500 1.575	
Help	OK Cancel	



SmartPower Operating Modes

Using SmartPower Modes and Scenarios

- What is a Mode in SmartPower?
 - It is a way to save a set of parameters defining the power of a design
 - You can create modes to record:
 - Operating Conditions: Specific Temperature or Voltage Settings
 - Activities: Different simulations, or turning one clock Off...



- We also offer predefined Modes:
 - Flash*Freeze
 - Sleep
 - Stand-by (Fusion Only)



Using SmartPower Modes and Scenarios

- What is a Scenario in SmartPower?
 - It is a way to combine different modes to estimate the power over the life of a design, and not just in one mode
 - You can create Scenarios:
 - If you want to mix different simulations
 - If Operating Conditions are changing over the life of a Product
 - Temperature profile for Automotive
 - Voltage variations due to battery decay
 - If you want to mix different modes (Flash*Freeze and Active)
 - We also offer predefined Scenario:
 - 95% Flash*Freeze 5% Active
 - 80% Flash*Freeze 20% Active
 - 50% Flash*Freeze 50% Active



Using SmartPower Modes and Scenarios

1 top - SmartPower	
File Edit View Tools Simulation	n Help
Modes and scenarios 🔹 🗙	Summary Domains Manalysis RT2 Frequencies Rt> Probabilities
Pre-derined modes	
Static	Power Consumption
Elash*Freeze	Total 27.25 mW
Sleep	Static 0.048 mW
Shutdown	Dynamic 27.202 mW
Pre-defined scenarios	
50% Flash*Freeze	Breakdown Bu Tune
80% Flash*Freeze	
95% Flash*Freeze	Banks Static Power Usage
	L U.U14 mVV
	0.034 mW
	0.281 mW Cote
	4.283 mW
	Net
	[22.030 m/v]
	Operating Conditions : Typical
	Operating Conditions Value
	1 Junction Temperature 25 C
	Change Operating Conditions
	Pattern
	Davely
	Battery capacity 1000.00 mA*Hrs Set
New custom mode	Pattern Ma 44.027 Harrish
New custom scenario	Dattely ine 44.037 Hour(s)
All simulation files are processed	
Ready	Active 25.00 C 1.20 V Speed: STD

- Supports Analysis with all modes of use for the FPGA
 - Active
 - Shutdown
 - Flash*Freeze (IGLOO)
 - Sleep
 - Standby
- Summary tab supports analysis of any mode
- Use Combination of Modes to Create a Power "Scenario"



SmartPower Custom Modes

Click to create custom mode





Creating a Power Scenario

tan SmartDever		
File Edit View Teels Circulation		
Modes and scenarios • x	Summary	
Static	Power Consumption	
Flash*Freeze	Total 27.25 mW	
Sleep	Static 0.048 mW	
Shutdewn	Dynamic 27.202 mW	
New custom scenario		
80% Flash*Freeze	Breakdown By Type Show Chart C Grid	
95% Flash*Freeze	Banks Static Power Usage	Specify mode and
	0.014 mW/	Specify mode and
	Power - New Scenario	duration
		Total must - 100%
	Name:	10101111031 - 10078
	Duration (%) Mode	
	Decative 4 Shutdown	
	5 Sleep	
	1 0 6 Standby	
	2 7	
	3 8	
	9	
	Chang Total: 0 % (Left: 100 %) Delete entry	
	Batteriu Commontu	
	Batter	
New custom mode	Batter Help OK Cancel	
All simulation files are processed		
Ready	Active 25.00 C 1.20 V Speed: STD	

SmartPower Reports

SmartPower Power Reports

- SmartPower can Generate the Following Reports:
 - Power Report
 - Scenario Power Report
 - Cycle Accurate Power Report
 - Activity and Hazards Power Report
- Text or CSV (Comma Separated Value) Format
- Customize Power Report
 - Items to Include in Report
 - Breakdown by Instance
 - Limit Number of Included Instances
 - Specify Minimum Power Level for Inclusion in Report
- Options Button Invokes Preferences Window



SmartPower Power Report Options





Power Report

TDMA32_WRP - Pow	ver Report							
File Actions Help	,							
Power Report for	design TDMA3	2_WRP with the	following sett	tings:				×
Vendor: Actel Program: Actel Date: Mon C Version: 3.0	l Corporation L Designer So Oct O9 12:14:	ftware, Releas OO 2006	≘ 7.2 SP1, Copy	yright (C	C) 1989–20	06		
Design: Family: Die: Package: Temperature: Voltage: Speed Grade: Operating Condit Power Mode:	TDMA Axce RTAX 352 MIL -1 cions: Typi Acti	32_WRP lerator 2505 CQFP cal ve						
Power Summary		++						
i i	Power (mW)	Percentage						
++	154.854	++ 100.0%						
Static Power	30.000	19.4%						
Dynamic Power +	124.854	80.6% ++						=
Breakdown by Rail ++	L Power (mW)	+	+ Current (mA)	-+ 				
+ Rail VCCA Rail VCCI 3.3	132.265 22.589	1.5 3.3	+ 88.177 6.845	-+ 				
Breakdown by Type		+	+ ⊇	-+				
+	+	+	+					
Type Net Type Gate	1 18.6	01 36.1 43 12.0	⊼ ≿					
Type I/O	21.9	29 14.2	\$					
Type Clock	28.4	01 18.3	\$					
Type Core Stati +	ic 30.0	00 19.4	k +					
Thermal Summary								
Ambient Temperat Junction Tempera Cooling Style: Thermal Resistar	cure: ature: nce Teta-JA:	25.0 C 27.1 C Still Air 13.5 C/W						


Power Report Breakdown by Instance

TDMA32_WRP - Pov	wer Report						
Actions <u>H</u> elp							
							~
ower Report for	design TDMA32	2_WRP with the	tings:				_
Vendor: Acte.	1 Corporation	D-1					
Program: Acce. Dete: Mon	1 Designer 503	rumare, Reieas 20 2006	pyright (C) 1989-2008				
Vergion: 30	000 09 12.19.2	.0 2000					
Verbion. 5.0							
. .							
Design: Familar	TDMAS	32_WRP					
ramily:	AXCE.	rator					
Dic. Deckere:	352 (
Temnerature:	МТІ.	5QFF					
Voltage:	MIL						
Speed Grade:	-1						
Operating Condi	tions: Typic	cal					
Power Mode:	Activ	ze -					
-							
ower Summary	+	+					
	Power (mW)	Percentage					
Total Power	154.854	100.0%					
Static Power	30.000	19.4%					
Dynamic Power	124.854	80.6%					
	+	+					
reakdown by Ins	tance						
				-+ Type	+ Power (mW)	+ Macro	+
PCI CLK					25.272		+
MAKE CLKS MAKE	H CLK			I/O	3.129	ADLIB:HCLKBUF	i
DP DONE pad				I/O	0.721	ADLIB:OUTBUF	i
WR_BE_NOW_pad[(0]			I/O	0.721	ADLIB:OUTBUF	Ì
WR_BE_NOW_pad[1]			I/O	0.721	ADLIB:OUTBUF	1
WR_BE_NOW_pad[:	2]			I/O	0.721	ADLIB:OUTBUF	1
WR_BE_NOW_pad[3]			I/O	0.721	ADLIB:OUTBUF	I
BARO_MEM_CYC_p	ad			I/O	0.719	ADLIB:OUTBUF	
BAR1_CYC_pad				1/0	0.719	ADLIB:OUTBUF	
BE_GNT_pad				1/0	0.719	ADLIB:OUTBUF	
				1/0	0.719	ADLIB:OUTBUF	- I
CONFIG_CYC_pad				1 1/0	1 0 340	ADI TD. OUTDUT	
DMA_GNT_pad				I/O		ADLIB:OUTBUF	



Scenario Power Report

- Create a Power Report Based on a Power Profile
 - Report shows where/how much power is consumed





Cycle Accurate Power Report Overview

- Feature Definition
 - Offers Peak Power Analysis from a Simulation (VCD) file
 - Allows Cycle by Cycle analysis of the Power over the simulation
- Why Cycle Accurate Power Report?
 - For critical applications, a cycle accurate report allows designing for worst-case scenario
 - A cycle accurate report allows simulation and analysis of power saving scenarios (example: clock with variable frequency)



Cycle-Accurate Power Reporting

- Accurate report of peak power per clock cycle
 - Based on testbench
- Cycle-by-cycle analysis of the power over the simulation
- Allows designing for worstcase scenario



Select Options

-Specify sampling period -Report format and results Actel Corporation Confidential © 2009



543

Cycle Accurate Power Report





Activity and Hazards Power Report

Feature Definition

- Allows the analysis of power dissipated by Hazards from a Simulation (VCD) file.
- Definition of Hazard: Due to the delay mismatch along different fanin paths of each internal gate, the output of a gate may have unexpected transitions before settling to the correct logic level. These transitions are called hazards or spurious transitions





Hazard Analysis

- Hazards can account for as much as 20% of total global power*
- Power dissipation caused by hazards can be much as 70% of total power

Fa IPU_IGLOO - Power_activity_and_hazards Report	_ O ×
Ble Actions Help	
Franky: 10400	
Deckers Add VBCA	
Temperature Deve - COM	
Voltage Bande : COM	
Overating Conditions : Twical	
Operating Hode : Active	
Data Source : Advanced	
Activity Map: Net Summary	
i Man i Clack Dennis i Tunn i Punntistan i Guaristan i Sunstana i Punntistan i Punntistan (2001) i Guaristan Danny (- NI - 1
Mec Clock Jomain Hype Junctional Pransitions Spirious Pransitions Junctional Power (mw) Spirious Power (m	24)
clk c clk Clock 40052 0 1.639 0.000	
output o pad[0]/00/NET1 clk Data 3938 1004 0.066 0.017	i
output_o_pad[1]/U0/NET1 clk Data 2709 1180 0.045 0.020	- i
underflow_o_pad/U0/NET1 clk Data 2631 610 0.050 0.012	
zero_pad/U0/NET1 clk Data 3171 40 0.061 0.001	
output_0_pad[2]/U0/NET1 clk Data 3066 526 0.051 0.009	
output_o_pad[5]/UU/NET1 Clk Data 3383 100 0.057 0.002	

- Report Highlights
 - # of functional transitions, # of hazards and their associated power

*According to Favalli and Benini, International Symposium on Low Power Electronics and Design, 1995



Activity and Hazards Power Report Options





Activity and Hazards Power Report Example 1

• For each net, report <u>activity</u>; sort by <u>spurious transitions</u>; sort order <u>descending</u>; Limit the number of reported nets to <u>50</u>.

FPU_IGLOO - Power_activty_and_hazards_1.	rpt Report						
Eile Actions Help							
Family : IGLOO Die : AGL600V5 Package : 484 FBGA Temperature Range : COM Voltage Range : COM Operating Conditions : Typical Operating Mode : Active Data Source : Advanced					We analyze the s per net, and we transitions and s	simulation report the spurious t	n cycle by cycle, and net e number of functional transitions for each net
Activity Map: Net Summary	+	+	+	+	+		
Net	Clock Domain	Type	Functional Transitions	Spurious Tra	ansitions		
<pre>+</pre>	<pre> clk /pre>	Data Data Data Data Data Data Data Data	4734 4407 4276 4912 4680 3952 3692 4506 4237 4470 4420 3284 4863 3660 4917 4498 4497 4498 4497 4735 3707 4227 2854 4521 4186 4510	<pre>32544 31992 31584 29008 28788 28754 28576 28116 27888 27818 27818 27818 27818 277126 27048 26676 26432 25196 24934 24468 24934 24468 24330 24238 24028 23504 23504 23058 22840</pre>	Functional Trans 4734 4407 4276 4912 4680 3952 3692 4506	sitions 	Spurious Transitions 32544 31992 31584 29008 28788 28754 28506 28116
<pre> 001/US/prod1_2[25] UUT/u5/prod1_2[21] UUT/u4/un1 exp in 4[3]</pre>	Clk Clk Clk	Data Data Data	4510 4163 4613	22840 21888 21856		1	



Activity and Hazards Power Report Example 2

• For each net, report <u>activity and power</u>; sort by <u>power</u>; sort order <u>descending</u>; Limit the number of reported nets to <u>40</u>.

e <u>A</u> ctions <u>H</u> elp 'amily : IGLOO												
Die : AGL600V5 Package : 484 FBGA Temperature Range : COM Voltage Range : COM Operating Conditions : Typical Operating Mode : Active Data Source : Advanced						We are also able to report functional power and spurious power for each each net						
ctivity Map: Net Summary	-+		+	+	+							
Net	Clock Domain	Туре	Functional Transitions	Spurious Transitions	Functional Power (mW)) Spu	rious	Powe	≘r (mW)			
<pre>clk_c clk_c output_o_pad[0]/U0/NET1 output_o_pad[1]/U0/NET1 underflow_o_pad/U0/NET1 clk_pad/U0/NET1 output_o_pad[2]/U0/NET1 clk_pad/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[12]/U0/NET1 output_o_pad[12]/U0/NET1 output_o_pad[12]/U0/NET1 output_o_pad[15]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[3]/U0/NET1 output_o_pad[6]/U0/NET1 output_o_pad[6]/U0/NET1 output_o_pad[6]/U0/NET1 output_o_pad[26]/U0/NET1 output_o_pad[16]/U0/NET1 output_o_pad[10/NET1 output_o_pad[10/NET1 output_o_pad[10/NET1 output_o_pad[11]/U0/NET1 output_o_pad[11]/U0/NET1 output_o_pad[12]/U0/NET1 output_o_pad[12]/U0/NET1 output_o_pad[12]/U0/NET1 output_o_pad[13]/U0/NET1 output_o_pad[13]/U0/NET1 output_o_pad[13]/U0/NET1 output_o_pad[13]/U0/NET1 output_o_pad[13]/U0/NET1 output_o_pad[13]/U0/NET1 output_o_pad[13]/U0/NET1 output_o_pad[13]/U0/NET1</pre>	<pre></pre>	Type Clock Data Data Data Data Data Data Data Dat	40052 3938 2709 2 831 3171 3066 3383 20026 3118 3078 3057 2896 2775 2915 2662 2676 2526 2676 2526 2676 2526 2676 2526 2676 2526 2676 2526 2676 2527 2629 2618 2556 2417 2428 2142 2084 1994	> Jourious Transitions 0 1004 1180 610 40 526 1004 1180 158 158 158 158 158 160 255 60 20 80 216 336 100 140 180 216 336 100 140 80 216 336 100 140 80 98 80 98 80 98 80 118 176	1 1.839 1 1.839 0 0.066 0 0.045 0 0.050 0 0.051 0 0.052 0 0.051 0 0.051 0 0.051 0 0.051 0 0.051 0 0.051 0 0.051 0 0.048 0 0.048 0 0.048 0 0.048 0 0.042 0 0.043 0 0.042 0 0.043 0 0.043 0 0.043 0 0.041 0 0.041 0 0.041 0 0.041 0 0.035 0 0.031		0.1003 000 117 120 1212 1212 1212 1212 1212 1212 1212 1212 1212 1212 1212 1212 1212 1212 1213 1214 1215 1215 1216 1217 1217 1218 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 1219 <	+	Functional 1.839 0.066 0.045 0.050 0.061 0.051 0.057 0.057 0.053	Power	(mV)	<pre>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>></pre>
UUT/u4/f2i_shft[3]	clk	Data	3625	5492	0.013	10.0	19	1	0.052			0.003
output_o_pad[30]/UO/NET1	clk	Data	1 1704	80	0.029	0.0)01					
UUT/u4/shift_left[1] ine_o_pad/UO/NET1	clk clk	Data Data	3996 422	2572 1010	0.017 0.007	0.0 0.0)11)17		Ì			



Programming & Debugging





Generating Programming File





Hands-on Labs 7, 8 and 9

- Complete Labs 7, 8 and 9 in the Lab Guide
- Lab 7
 - Layout Design
 - Generate Global Usage Report
 - Create backannotated timing file
 - Save your Work
- Lab 8
 - Run Post-layout timing simulation
 - Create VCD file
- Lab 9
 - Measure Power Consumption with SmartPower
 - Generate the programming file



Programming

Sculptor 3 Overview

- PC-based Parallel-port, Single Device Programmer
- Replaces Silicon Sculptor II
- Compatible with all Sculptor II Adapter Modules
- Supports all Devices and Families:
 - IGLOO/e, Fusion, ProASIC3/E, ProASIC^{PLUS}
 - ARM-enabled Flash FPGAs
 - All anti-fuse products including RTAX4000S





Actel Corporation Confidential © 2009

Silicon Sculptor Software

- Available from Actel Website
 - http://www.actel.com/custsup/updates/silisculpt/
- Requirements (Windows Version)
 - Microsoft Windows 95/98, Win NT or Win 2000
- Requirements (DOS Version)
 - 286 with 4MB RAM, Approx. 6MB Hard Drive Space
 - DOS-driven Program Memory Managers Not Required
 - DOS Shell from Windows 95/98 OK
 - Does Not Work with Windows NT



Flash Programming

Flash FPGA Devices Can Be Programmed Multiple Ways

- Off-board Programming with Silicon Sculptor 3
- In-System Programming (ISP) using JTAG Interface with:
 - Silicon Sculptor 3 (ProASIC, ProASIC^{PLUS}, ProASIC3/E, Fusion, IGLOO/e)
 - Flash Pro (ProASIC or ProASIC^{PLUS})
 - Flash Pro Lite (ProASIC^{PLUS})
 - Flash Pro 3 (ProASIC3/E, Fusion, IGLOO/e)
- Programming via Microprocessor Interface
 - (ProASIC^{PLUS}, ProASIC3/E, Fusion, IGLOO/e)



FlashPro Programmer ProASIC, ProASIC^{PLUS}

- Small Form Factor 24 in³
- Low Cost
- Hardware Features
 - Small 26-pin Header
 - Samtec FTSH-113-01-L-D-K
 - 20" Ribbon Cable
 - ECP Parallel Port
- Software Features
 - Win 95/98/NT/00 O/S
 - STAPL Support
 - Daisy Chain Capability
 - Log File Generation
 - Self-test Option



2.5/3.3V	1	2	VDDP
2.5V/3.3V	3	4	VDDP
2.5V/3.3V	5	б	VPP
GND	7	8	VPN
GND	9	10	GND
GND	11	12	TCK
NC	13	14	TDI
NC	15	16	TDO
GND	17	18	TMS
GND	19	20	RCK
TRSTB	21	22	TRSTB
2.5V	23	24	VDDL/VDD
2.5V	25	26	VDDLVDD



FlashPro Lite Programmer ProASIC^{PLUS}

- Low Cost
- Ultra-small Form Factor
- Hardware Features
 - Draws Power from Target Board
 - Connects to Parallel Port
 - Supports In-system Programming
 - Samtec 26-pin Header
- Software Features
 - Supports Windows 98, NT, 2000, and XP Operating Systems
 - STAPL Support
 - Free Software Updates





FlashPro 3 ProASIC3, ProASIC3L, Fusion and IGLOO

- USB 2.0 High-speed Interface
 - 10-pin JTAG ISP
 - Altera-compatible Interface
- Programs ProASIC3 Devices in Less than 2 Minutes
- Powered by USB Connection
 - Parallel Programming Requires Powered USB Hub
- Variable TCK (up to 24 MHz)
 - Recommend <= 20MHz for PA3/E
- Optional Transition Board provides Adapter Cables for 26- and 10-pin SAMTEC







Programmer Summary

Programmer	Device Support	Availability
	All antifuse FPGAs	
	ProASIC3/E, ProASIC3L, Fusion, IGLOO/e	
Silicon Scupltor 3	ProASIC and ProASIC ^{PLUS}	Available
FlashPro	ProASIC and ProASIC ^{PLUS}	Available
FlashPro Lite	ProASIC ^{PLUS}	Available
FlashPro 3	ProASIC3\E, Fusion, IGLOO/e	Available



FlashPro 8.5

FlashPro v8.5 Software Overview

- Works with all FlashPro series programmers
 - FlashPro3, FlashPro Lite and FlashPro
- Supports A500K, APA, ProASIC3/E/L, AFS and AGL with appropriate programmer
 - ProASIC3/E/L, AFS and AGL support via FlashPro3 only
- Allows programming in parallel via USB hubs
 - Huge increase in throughput for small-scale production
 - FlashPro3 and FlashPro can be operated in parallel
- Supports Chain Programming
- Supports Device Serialization



FlashPro User Interface





Programming with FlashPro

- Launch FlashPro
- Load STAPL File
- Select Action
- Execute Action



Invoking Programming Software from Libero

Click "Programming" in Project Flow Window or...



FlashPro GUI

- Select Configure Device File to Display Programming File
 - Single File Configuration Window is Displayed





FlashPro Select Action and Execute Action

Select Action to Perform from Pull-down Menu





 Programmer Status is Displayed in Programming List Window





FlashPro Programming Complete

Successful Programming is Indicated in the Programmer Status Column





FlashPro Connecting Multiple Programmers

 FlashPro 8.5 Supports Connecting Multiple Programmers To One Computer

🕌 FlashPro - [TOP] *				
<u>File Edit View Tools Programmers Configuration Cus</u>	sto <u>m</u> ize <u>H</u> elp			
🗅 🖙 🖬 🤶 🐗 🏟 🏟 🛸 📾 🖼	i 🦚 🚓			
New Project 1	Configure Device		PROGRAM	
* Programmer Name 1 06426	Programmer Type FlashPro3	Port usb06426 (USB 2.0)	Programmer Status	Programmer Enabled
Scan for programmers	Refresh/Rescan for P	rogrammers	Sele	ct or de-sele
programmer '06426' : FlashPro3 programmer '05265' : FlashPro3 Rescanning for Programmers DONE.	2		prog	
All / Errors / Warnings / Info /				
				and the second se



Parallel Programming

Parallel Programming

Operation/Production Programming

• Programming multiple Flash devices using single GUI





Parallel Programming (cont)





Chain Programming

Overview

Why Chain Programming?

• We want to program Actel devices with non-Actel devices in the same JTAG chain

First device - TDO

connects to the programmer

• Devices are programmed in sequential order



Last device - TDI connects to the programmer
Chain Programming

- Steps:
 - Create a FlashPro project
 - Specify Chain Programming
 - Configure the Chain
 - Select Programming file for device(s) to be programmed

New Project	
Project <u>N</u> ame:	
Prog_chain	
Project Location:	
C:\Actelprj\Chain_test\Prog_chain	Browse
Programming mode	
C Single device	
OK Cancel	Help

- Select BSDL file for device(s) to be bypassed
 - Can manually enter IR length and maximum TCK rate
- Program Chain



Chain Programming Automatic Chain Configuration

Configuration > Construct Chain Automatically

	F	lashPro -	[Prog_chain]					
Fi	е	Edit View	Tools Programmers	Configuration Custo	omize Help			
<u>]]</u>			New Project Open Project	Add Actel Device Add Non-Actel De Add Actel Devices Construct Chain	Ctr avice Ctr s From Files Ctr Automatically View Programm	+Shift+T +Shift+N +Shift+F ers	RUN	
×	Γ		Programmer Name	Programmer Type	Port	Programmer Status	Programmer Enabled	Device / Action
ammer List Window		03263		FlashFro3	Befresh/Bescan fr	r Programmers	<u>v</u>	
× Progra					Heneshiritesedine			
	•		Errors λ Warnings λ	Info /				
	net#	uct the devi	ice chain automatically fro	m a Scan Chain oper	ation		Ni	o devices in chain [CHAIN]
0	nsu	accure devi	ice chain automatically fru	in a scan chain uper	auon		DIC DIC	



Chain Programming Manual Chain Configuration

Manually Add Devices from Configuration Menu

F F	lashPro - [Prog_chain] *								
Eile	Edit View Iools Programmer	S Configuration Custo Add Actel Device.	<u>mize Help</u>	itrl+Shift+T trl+Shift+N	** **	\$\$ \$ \$			
	New	Prc Construct Chain A	Automatically	trrt+Shift+F		→ [RUN	BUN	
N N N	TD I N TD0 → +++ → TD I 2 Show Chain Editing			Configuration	Configure	Device	<u>+</u> <u>+</u>	Add Act	tel Device 🔀
on Wind	Device	Name	File	IR Length	Max TCK (MHz)	Enable Device	Enable Serial	Action	Serial Data
Chain Configurat	Construct the chain from	<u>ı a Scan Chain ope</u>	ration						
*									
1113	I FILLAN A EFFORS A WARDINGS	0 1000 (



Manual Configuration Adding a Device

Add Actel Device	
File Programming file:	
C Device	ОК
	Cancel
Name :	Help

Add Non-Actel Device	
File BSDL file:	
C Data IR length: 2 Max TCK Freg.: 1 MHz	ОК
	Cancel
Name: Non Actel Device	Help

Actel Device

- Select Programming file
- User can specify custom name

Non-Actel Device

- User can select BSDL file
 - Provides the Max TCK Frequency and IR length for device
- User can enter data directly if they do not have access to a BSDL file
- User can enter custom name for device



Configured Chain





Programming the Chain

FlashPro - [Prog_	chain] *								
<u>File E</u> dit <u>V</u> iew <u>T</u> ools	Programmers	<u>C</u> onfiguration Custo <u>m</u>	nize <u>H</u> elp				1.00		
0 🚅 🖬 🤶	-	22 22 E	🥸 🦔 🎊		\$\$\$ \$\$\$	\$0 st		\$	
	New Pro	oject 🎦	View	ïgure Chain	\$	→	RUN		
×→TDI N TDO→++	•	Do→TDI 1 TDO-		Configuration	Config	ure Device		Add	Actel Device 🔀
3 Device	e	Name	File	IR Length	Max TCK (MHz)	Enable Device	Enable Serial	Action	Serial Data
Device 1 AFS600	e AFS	Name 6600	File D:\Actelprj\	IR Length 8	Max TCK (MHz) 10	Enable Device	Enable Serial	Action PROGRAM 💌	Serial Data
Bevice 0 2 A3P250 0 2 A3P250	e AFS	Name 6000 P(LIN)/AGL(N)250(Z)	File D:\Actelprj\	IR Length 8 8	Max TCK (MHz) 10 10	Enable Device	Enable Serial	Action PROGRAM PROGRAM	Serial Data
AFS600 2 A3P250 Ultrophysical actions of the second seco	e AFS	Name ;600 *(LIN)/AGL(N)250(Z)	File D:\Actelprj\ C\Actelprj\	IR Length 8 8	Max TCK (MHz) 10 10	Enable Device V	Enable Serial	Action PROGRAM 💌 PROGRAM 💌	Serial Data
Device Device 2 A3P250 X	e AFS	Name 5600 *(LIN)/AGL(N)250(Z)	File D:\Actelpri\ C:\Actelpri\ C:\Actelpri\.	IR Length 8	Max TCK (MHz) 10 10 Seleo	Enable Device	Enable Serial	Action PROGRAM PROGRAM	Serial Data
Device Device 1 AFS600 2 A3P250 Viet All Errors	e AFS ☑ A3F	Name 600 (LIN)/AGL(N)250(Z) Info /	File D:\Actelprj\ C\Actelprj\	IR Length 8	Max TCK (MHz) 10 10 Seleo	Enable Device	Enable Serial	Action PROGRAM PROGRAM S) to pro	Serial Data



Programmed Chain

🕼 FlashPro - [Prog_chain] * File Edit View Tools Programmers Configuration Customize Help **S R M** New Project Configure Chain RUN d'h P Open Project View Programmers Programmer Programmer Programmer Programmer **Device / Action** Port Enabled Name Туре Status 3 List 1 05265 FlashPro3 usb05265 (USB 2.0) RUN PASSED 5 A3P250/PROGRAM Refresh/Rescan for Programmers programmer '05265' : device 'AFS600' : Executing action PROGRAM programmer '05265' : device 'AFS600' : Checking for Backup Calibration Data... programmer '05265' : device 'AFS600' : Reading Master Calibration Data... programmer '05265' : device 'AFS600' : Writing Calibration Backup Copy programmer '05265' : device 'AFS600' : Erase ... programmer '05265' : device 'AFS600' : Completed erase programmer '05265' : device 'AFS600' : Programming FPGA Array programmer '05265' : device 'AFS600' : Verifying FPGA Array programmer '05265' : device 'AFS600' : Verifying FPGA Array -- pass programmer '05265' : device 'AFS600' : Finished: Thu Feb 05 13:25:27 2009 (Elapsed time 00:01:12) programmer '05265' : device 'AFS600' : Executing action PROGRAM PASSED. * _ * _ * _ * _ * _ * programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Executing action PROGRAM programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Erase ... Warning: programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Cannot save file: 'C:\Actelprj\Chain test Please check the write permission. programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Completed erase programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Programming FPGA Array programmer '05265' : device 'A3P(L|N)/AGL(N)250(2)' : Verifying FPGA Array programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Verifying FPGA Array -- pass programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Program FlashROM ... programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Verify FlashROM ... programmer '05265' : device 'A3P(L|N)/AGL(N)250(Z)' : Verify FlashROM -- pass ADDITING (ACTING FOIRLE . REALENEY. The Ret OF 40.00.40 All (Errors) Warnings) Info) 2 devices in chain CHAIN Ready

Messages indicate status of each device to be programmed



Device Serialization

Device Serialization: STAPL File Format

When Using FROM with Serialization Feature

• User can select the target programmer

FlashR	DM re	gion	s:														Region_7_0	
m words	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Properties:	
pages							-	-		-	_		_	_		_	Name	Region_7_0
7																	Start page	7
	17																Start word	0
°																	Length	16
5																	Content	Auto Inc
	<u>-</u>																Start value	0
4																	(HEX)	14
3	177																Step Value (HEX	1
																	Max value (HEA)	
2																		
4	1-																1	
<u> </u>																		
0																		
ROM prog	rammir xrograr	ng fil mmin	e typ ng file	e e for a	all de	evice	s					0 (One	prog	ramn	ning	file per device	
ROM prog Single p or of device	rammir xrograr xs to p	ng fik mmin rogra	e typ ng file am:	e —	all de	evice	es 10					0 (One	prog	ramn	ning Targ	file per device	
ROM prog Single p er of device	rammir xrograr xs to p	ng fil mmin rogra	e typ ng file am: Ty f	e for:	all de	evice	es 10					0 (One	prog	ramn	ning Targ	file per device	
ROM prog Single (r of device Progra	rammin program es to p mm	ng fil mmin rogra er	e typ ng file am: Typ	pe	all de	evice	es [10					0(Dne	prog	ramn	ning Targ	file per device	Cancel
ROM prog Single r of device Progra ogramn	rammir program ss to p mm ier ty	ng fil mmin rogra er	e typ ng file am: Typ	pe e for ; pe	all de	evice	es [10						One ;	prog	ramn	ning Targ	file per device	Cancel
OM prog Single (of device rogra ogramn	rammir progran es to p mm er ty ric S	ng fil mmin rogra pes TAI	e typ ng file am: Typ	pe pe	all de	evice	es [10					0 (Dne	prog	ramn	ning Targ	file per device et Brogrammer	Cancel
OM prog Single (of device Program Ogram Gene	rammir program is to p ier ty ric S	ng fil mmin rogra pes TAI	e typ ng file am: Typ PL p	pe pe	all de	evice	es 10						Dne	prog	ramn	ning	file per device et Brogrammer	Cancel
ROM prog Single er of device Program 'rogramn Gene Silico	rammii orograi istop ier ty iric S n Sc	ng fik mmin rogra pes TAI	e typ ng file am: Typ PL p tor I	pe play	er PA	evice	es [10	ogra		her,	or F	O (Dine (prog	ramn	ning Targ	file per device et Brogrammer	Cancel

STAPL Serialization

- For Silicon Sculptor II or Sculptor 3, BP Auto Programmer or FlashPro3
- Actel and BP specific STAPL format to support device serialization
- Auto Serial Index
 Increment

Generic STAPL Player

• Each FROM and ARRAY content has its own action



Device Serialization: STAPL File Format





Serialization Options

- What Should Happen when Programming fails on a Single Board with one Device?
 - User has GUI option in FlashPro to
 - Reprogram same serial number (Reuse)
 - Program with the next sequential number (Skip)











Debug Tools

FPGA Debug Tools

- Identify AE
- Silicon Explorer II



What is Identify AE?

RTL Source Level Hardware Debugger from Synplicity

- Allow internal visibility in the target system at full speed
- Trigger on data path and control path
- Instrument and Debug Design directly in RTL source code
- View data in standard waveform display





Identify AE Product Specification

- Supported Devices
 - Identify AE v3.0.2A: ProASICPLUS, ProAsic3, Fusion and IGLOO
- Supported Programmers:
 - FlashPro, FlashPro Lite and FlashPro3
- HDL Language Support
 - VHDL, Verilog or mixed language designs
- FREE 1 year License



FPGA Debug Tools

- Identify AE
- Silicon Explorer II



Silicon Explorer

- Debug Antifuse Designs in Real Time!
 - Select Internal FPGA Nodes on the Fly for Viewing while Device Runs at FULL Speed!
 - Reduce Debug Time and Decreases Time to Market!







Action Probe Circuitry

- Dynamic Internal Node Access
 - No Changes to Timing Relationships
 - No Changes to Fan-out or Node Loading
- Patented Architectural Feature
 - Antifuse Devices Only
 - Unique to Actel
- No Silicon Overhead
 - Uses Zero Logic Resources
 - Always there if Needed





Summary

- Libero FPGA Design Suite Includes:
 - Design Entry
 - ViewDraw, HDL Editor, SmartGen, SmartDesign
 - Synthesis
 - Synplicity
 - Verification
 - ModelSim, WaveFormer Lite
 - Designer (P&R, Timing Analysis and Constraints)
- Actel Continues to Improve Libero IDE
 - Increased Quality of Results
 - Ease of Use
 - Additional Features





Reference Material

Reference Material

- SmartGen
- ViewDraw
- CoreConsole
- WaveFormer Lite
- ModelSim Dataflow and List Windows
- Synplify Attributes and Directives
- Chip Editor
- SDC Timing Constraints
- Silicon Sculptor
- Device Serialization



SmartGen

SmartGen RAM Initialization

- Speeds Simulation Time by Reducing the Initial Writes to Setup the Memory
- Completely Automated Simulation Flow
- MEMORYFILE Property Preserved Throughout the Design Flow
- Cascading of Multiple RAM Blocks Handled Automatically
- Supports Industry Standard Memory Content Specification Files





SmartGen RAM Initialization ProASIC3 and Axcelerator (cont.)

RAM : Create Core		Customize RAM Content
Write Depth 1 Write Width 1	Read Depth 1	RAM Configuration Write Depth: 1 Write Width: 1 Read Width:
 Single Read/Write Clock Independent Read and Write Cloc 	<s< td=""><td>Write Port View Read Port View Go To Address:</td></s<>	Write Port View Read Port View Go To Address:
Write Clock © Rising © Falling RAM Type © Two Port © Dual Port Write Enable © Active Low	Read Clock C Rising C Falling Reset Active Low Active High None Read Enable C Active Low	O Go Address HEX Data HEX
C Active High	Active High Read Pipeline B Write Mode B	
C Retain Output Data	C Retain Output C Pass Write D Customize RAM Content Vepping Help Close	e Default Data 0 Reset all values I Import from file
		Help OK Cancel



Memory Content Manager - Features

- Variable Aspect Ratio Support
 - Read View & Write View
- Import of User Memory File
 - Intel hex format
 - Motorola- S format
- Multiple Radix for Data and Address Display
 - Hexadecimal
 - Binary
 - Decimal

RAM Configuration	
Write Depth: 4096	Read Depth: 2048
Write Width: 4	Read Width: 8
· · · · · · · · · · · · · · · · · · ·	, ,
Write Port View Read Port View	
Go To Address:	
0 <u>Go</u>	
Address HEX 🔻	Data BIN 💌
0	1010
1	1010 🗖
2	0000
4	1010
5	1010
mize RAM Content	
AM Configuration	
Write Depth: 4096	Read Depth: 2048
111-26-112-466 · 4	Deeduurahk.
write width:	Read width: 10
Vrite Port View Read Port View	
Go To Address:	
0 Go	
1	01010000
2	10101010
3	10101010
	10101010
6	10101010
7	10101010
8	10101010
9	10101010
A	10101010
	10101010
	10101010
	10101010
E	10101010
E	10101010
E F 10	10101010 10101010 10101010
E F 10 11	10101010 10101010 10101010 10101010
E F 10 11	10101010 10101010 10101010 10101010
E F 10 11	10101010 10101010 10101010
E F 10 11	10101010 10101010 10101010



SmartGen Soft FIFO Controller

Create Controller With or Without Memory

Soft FIFO Controller with	Memory : Create Core	
Write port Depth: Width:	DATA WE Allow write when FIFO is full AFULL AFULL	
Single clock		
Read port Depth:	RCLOCK	→ → □
Width:	DVLD UNDERFLOW RDCNT	
Help		nerate Close



ViewDraw

Adding Schematic Border

- Built-in Library Contains Several Sheet Border Templates
 - Templates Can Be Modified





ViewDraw Border in Schematic





Customizing a Schematic Border

- Border Template Can Be Customized
- Open Border (File > Open)
 - Select Symbol from "Type" Menu





Customizing a Schematic Border (cont.)

Save File to New Name

- (File > Save Copy As <name>)
- Border Saved in Project Library
 - Visible on Libero File Manager Tab





Customizing a Schematic Border (cont.)

 Open Saved Border and B Add Lines, Arcs, Text, etc. Mathematic Viewdraw act_bsheet 1 OK OxActelpri/Schematic file act_bsheet 1 	Edit (File > Open) as Necessary Modified border visible on File Manager tab	 Project Design Files Block Symbol Files act_bsheet.1 Schematic Files HDL Source Files SmartGen Cores CoreConsole Project Designer Block Stimulus Files Constraint Files Synthesis Files Physical Synthesis Files Designer Views Impl1 (designer\impl1)
(actelcells) (builtin)	sym\actl_bsheet	Design Hierarchy File Manager
Symbol Project Directory: D:\Actelprj\Schematic_files\my_schematic\viewdraw		



CoreConsole

CoreConsole IP Deployment Platform



- System-level Design Builder
 - Fast assembly and configuration of user designs
 - Easy to use graphical user interface
- Incorporated IP Delivery
 - Users can access IP modules in the IP Vault
 - Some modules require a separate license
- System Output
 - Configured RTL can be either plain text or obfuscated
 - CoreMP7 and other protected IP output as a blackbox
 - Output includes
 - System and IP test benches
 - Memory map generation with software driver export



CoreConsole/Libero IDE Design Flow





Opening CoreConsole

- Click CoreConsole Button in Project Flow Window
- Add and Stitch Components
- Generate IP






CoreConsole v1.4 User Interface



Add Components



CoreConsole v1.4 GUI Tabs





CoreConsole v1.4

 Automatic Detection or Manual Check For New/Updated Cores

System Options	
	CoreConsole - IP Cores Available
General Updates	IP Cores Available for Download Details
Checking	Downloaded - Core16550 v3.0.128 1.17 MB 💽 CoreConsole - IP Database
Automatic: Automatically download and install cores	✓ Downloaded - CoreRSENC v2.0.179 0.63 MB ① You have connected to the server for the
⊙ Standard: Check for Updates on startup	CortexM1 v2.1.105 38.93 MB (1) CoreConsole IP database.
O Manual: No automatic check	Core List on Server: Last updated: 2007-11-09 18:11:27
Update Now	
Internet	Bytes read 19988480 of 38928386 for IP core:
URL: www.actel.com/dataex	Actel_DirectCore_CortexM1Top_2.1.105.ccz
CoreConsole - test	
File View Actions Option	ODS Help
	Get List - Fetch list of additional IP cores available
Componen Auto Lavoul	✓ - Most recent versions only, when fetching list
- Calast	
Auto Stitch.	T T T I I I I I I I I I I I I I I I I I
	To Top Level Select All/None Hide
Check for U	Jpdates
OK Can Add To Data	
Rebuild Data	:abase



CoreConsole v1.4 Add Components

- Components Tab Lists Available Components
- Push Button to Add Component
- Multiple Instances of the Same Core Are Given Unique Names in Schematic

Components	
Selected Component's Details	
CoreAPB The CoreAPB controller implements an AMBA APB fabric with the same implementation model as the CoreAHBLite controller. The CoreAHB2APB bridge does the actual address decoding and SEL generation so primarily what this component does is the PRDATA multiplexing. There is one APB Master interface which is typically connected to the CoreAPB bridge and 10 APB atom interface. The Version 1.0 Add Components available for selection Listed: 34 of a total of 169 components	Push button to ADD
Processors, Actel	
Core8051s	
CoreABC	
CoreMP7	
Bus Interfaces, Actel	
Core429	
CoreAHB	
CoreAHB2APB	
CoreAHBLite	
CoreAPB	List of available cores
CoreAPB3	
CoreMP7Bridge	
Peripherals, Actel	
Core10100	
Core10100_AHBAPB	
Core1553BRM	
Core1553BRT	
Core429_APB	



Generate





CoreConsole Project in Libero





WaveFormer Lite

WaveFormer Lite
e Export Edit Bus ParameterLibs Report View Options Window Help
🖆 🖬 🗿 臍 🎒 🍳 Q, Q, Q, Q
Lagram - ram8x8.tim*
Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Q - Q R
240.0ns 28.00ns 170ns 180ns 190ns 200ns 210ns 220ns 230ns 240ns 250ns
DI[7:0] F7 X EF X DF X BF X 7F X 55 X AA X
WADD[2:0] 1 X 0 X 0 X 1 X 2 X 3 X 4 X
RADD[2:0]
DO[7:0]
Simulation Inactive



💁 WaveFormer Lite
File Export Edit Bus ParameterLibs Report View Options Window Help
Cragram - ram8x8.tim*
Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Q + Q F Add Clock Add Spacer Hold Text Marker Image: Constraint of the setup Image: Constrainton of the setup Image
240.0ns 28.00ns 170ns 180ns 190ns 200ns 210ns 220ns 230ns 240ns 240ns 250ns
DI[7:0] F7 X EF X DF X BF X 7F X 55 X AA X
WADD[2:0] 1 X 0 X 0 X 1 X 2 X 3 X 4 X
RADD[2:0]
DO[7:0]
Simulation Inactive



Ø w	/aveForn	ner Lite													<u> </u>
File	Export	Edit Bus	ParameterLibs	Report	View	Options	Window	Help							
🚘		Undo Zoo	>m		Ctr	Ί+Ζ									
Ľ.		Redo			Ctr	'+Υ									
1 init	Diagram	Delete			De	I									
Add Add	Signal Ad Clock Ad	Clear Red	Events				<u> </u>	HEX €	<u>q</u> + <u>q</u> <u>q</u> - <u>q</u>	F R					
180	.0ns <mark>32</mark>	Copy Ole	Image To Clipbo View To Clipboa	bard \wisa ard \wisave	ve		s 210)ns II	220ns	S I I I	230ns	24	10ns	250ns	
⊫		Copy To (Clipboard	i a (n 5an				<u> </u>		<u> </u>		<u> </u>		<u> </u>	_́≜
⊢		Cut Signal	ls/Text		Ctr	·l+Χ			_/	75					╗╢
		Select All S	Signals		Ctr	1+A		-	<u></u>	-	<u>_/</u>			~~	
	WAD	Copy Sign	nals		Ctr	1+C	X	1	_X	2	_X	3	X	4	<u> </u>
	RAD	Paste Sigr	hals		Ctr	' +V									
	E	Block Cop	y Waveforms												
1		Edit Clock	Ser e												
1		Insert Clo	ck Cycles												
		Delete Clo	ock Cycles												
		Right Click	< Delete Mode												
Co	pies th	Edit Text. (Un)Loc k	 Edges of Selecte	ed Signals		×	signals			Simu	Ilation	Inactive	9		▼



WaveForn	ner Lite		Choose the Start, End, Plac
File Export	Edit Bus ParameterLibs Repo	ort View Optio	Time C Clock Cycles
Diagram	Undo Zoom Redo Delete Clear Red Events	Ctrl+Z Ctrl+Y Del	Start: Ins
180.0ns 32	Copy Ole Image To Clipboard \v Copy Ole View To Clipboard \w Copy To Clipboard	w save save	Change Waveform Destinat
WAD	Cut Signals/Text Select All Signals Copy Signals	Ctrl+X Ctrl+A Ctrl+C	WADD
	Paste Signals Block Copy Waveforms	Ctrl+V	
•	Edit Clock Insert Clock Cycles Delete Clock Cycles Right Click Delete Mode		
Copies the	Edit Text (Un)Lock Edges of Selected Sign	nals	ОК





WaveForr	mer Lite			Choose t	ne Start, End	d, Place
File Export	Edit Bus ParameterLibs	Report View	Optio	© Time	C Clock C	ycles
🕞 🖬 🎒 🛛	Undo Zoom Redo Delete Clear Red Events	Ctr Ctr De	'l+Ζ 'l+Υ Ι	Start: End:	0	ns ns
Add Clock Add	Copy Ole Image To Clipbo Copy Ole View To Clipboar Copy To Clipboard	ard \w save d \w save		Place At: Change V WADD	1100 Vaveform De	ns estinatio
WA	Cut Signals/Text Select All Signals Copy Signals	Ctr Ctr	1+X 1+A 1+C	WADD		
RA	Paste Signals Block Copy Waveforms	Ctr	' +∀			
	Edit Clock Insert Clock Cycles Delete Clock Cycles Right Click Delete Mode					
Copies the	Edit Text (Un)Lock Edges of Selecte	d Signals	1		ОК] _





Signal Can Be Copied

🖉 WaveFori	ner Lite		Choose the Start, End, Place /
File Export	Edit Bus ParameterLibs Report	View Optio	C Time C Clock Cycles
Add Signal Ac	Undo Zoom Redo Delete Clear Red Events	Ctrl+Z Ctrl+Y Del	Start: 0 ns End: 1100 ns
180.0ns 32	Copy Ole Image To Clipboard \w sa Copy Ole View To Clipboard \w save Copy To Clipboard	ve 3	Change Waveform Destination
 WAI RAI	Cut Signals/Text Select All Signals Copy Signals Paste Signals	Ctrl+X Ctrl+A Ctrl+C Ctrl+V	WADD
[Block Copy Waveforms		
•	Edit Clock Insert Clock Cycles Delete Clock Cycles Right Click Delete Mode		
Copies th	Edit Text (Un)Lock Edges of Selected Signals		OK

? × Block Copy Waveforms At units -Controlling ⊙ Insert O Overwrite # of Copies: 1 250ns RADD • RADD Help Cancel



👱 WaveFormer Lite
File Export Edit Bus ParameterLibs Report View Options Window Help
CDiagram - ram8x8.tim*
Add Signal Add Bus Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Add Clock Add Spacer Hold Text Marker Image: Control of the setup in
184.0ns <mark>28.00ns</mark> 170ns 180ns 190ns 200ns 210ns 220ns 230ns 240ns 250ns 1
DI[7:0] F7 (EF (DF (BF (7F (55 (AA)
WADD[2:0] 1 (0 (0 (1) 2) 3 (4)
[RADD[2:0] 1 (0 (0 (1 (2 (3 (4))))))
DO[7:0]
Copy of waveform
is inserted!
Left click for Sample Mode (right mouse draws samples on diagram), right clic Simulation Inactive



Reactive Test Bench: Stimulus and Expected Response

- Draw stimulus waveforms on the input ports of the model under test.
- Draw expected response waveforms on the output ports of the model under test

	🕂 Diagram	- untitled0).btin	n*												_	
	Add Signal	Add Bus		Delay	Setup	Sample	HIG	ih Low	TRI	VAL	INVal	WHI	WLO	HEX		+ Q F	
l	Add Clock	Add Spacer		Hold	lext	Marker				Ψ		2	<u>~</u>		Q •	- 9, R	
l	141.0ns	-98.00ns	Ons	;		50	ns L		100r	IS	1	150r	ns I I		200ns		25
		Request											/				
		Grant															



Reactive Test Bench: Samples

- Samples Verify MUT Output
 - Sample constructs can monitor and perform actions based on the data sampled
 - Sample can work at a single point or over a windowed area
 - Sample can perform relative to the beginning of the transaction or relative to another event in the diagram.





Reactive Test Bench: Control & Looping

- Markers used for Control & Looping Sections of Transactions
 - Specify the end of the transaction
 - Create loops using for, while, and repeat loop markers
 - Insert HDL code

🕂 Diagram - loopdiag	ram.btim									
Add Signal Add Bus Add Clock Add Spacer	Delay S Hold	Setup Sample Text Marker	HIGH				_0 HE:	× • • •	Q.F Q.R	ViewVariabl Class Metho
3.072ns <mark>-355.8ns</mark>	Ons	, , 100	ns	200r	າຮຸ	300ns	•	400ns	1 1	500ns
		Çor Loop					Loop E	End		•
	F		УV	'hile Loop	Ţ	Loop End	1		End D	iagram 💻
СЦКО							۱		<u> </u>	
SIG0				varO						
SIG1					Va	r1				



Reactive Test Bench: Variables

- Variables Parameterize State Values
 - Variables can drive values on stimulus waveforms
 - Variables can store values on expected waveforms
 - Waveform states can be expressed as conditional expressions using variables

- Diagram ·	- reactive_	_variables.btim	_ 🗆 🗙
Add Signal 7 Add Clock 7	Add Bus Add Spacer	Delay Setup Sample HIGH LOW TRI VAL INVal WHI WLO HEX Q + Hold Text Marker	Q.F Q.R
164.0ns	52.00ns	Ons 50ns 100ns 150ns 200ns	
	CSB		▲
	WRB		
AE	3US[7:0]	(addr)	
DE	3US[7:0]	data	



Reactive Test Bench: Delays

- Delays Parameterize Time Values
 - Delays represent the time between two edges in the diagram
 - Specify min and max values
 - Delay values can be time or cycle-based
 - Conditionally control when edges occur

🕂 Diagram - re	Diagram - reactive_delays.btim								
Add Signal Add	d Bus	Delay Set	up Sample	HIGH LOW	TRI VAL	INVal WHI	WLO H	EX 🔍 +	Q.F.
Add Clock Ad	d Spacer	Hold Te	kt Marker		<u> </u>		~ ∢	<u> </u>	Q, R
24.00ns <mark>-64</mark>	.00ns	Ons	50ns		100ns	150n	IS I I I	200ns	
	CLK				<u></u>				<u> </u>
			└₊∣D	0		<mark>l</mark> ∎D1			
CSB									
WRB									
ABUS[7:0]		(addr)							
DBUS[7:0]		data							



Reactive Test Bench: Help Resources

- Online Manual:
 - Choose Reactive Test Bench Generation Under the Help menu
- PDF Manual:
 - Reactive_testbench_Generation_Option.pdf under the Help folder in the SynaptiCAD install directory
- SynaptiCAD's website: www.syncad.com



ModelSim AE

Dataflow Window

Explore physical connectivity of design

- Displays processes, signals, nets and registers
- Links to Main, Process, Signals, Wave and Source windows
- Find feature allows searching for signal, net or register names



wave - default

_ 🗆 🗙

Dataflow Window ModelSim AE Simulator

- The ModelSim AE simulator has a limited Dataflow functionality
 - Only one process and it's attached signals or one signal and it's attached processes are displayed





List Window

- Simulation Results in Tabular Format
 - VHDL Signals and Process Variables
 - Verilog Nets and Registers
- "Drag & Drop"
- Find Function
- Trigger / Strobe Properties
- Write List
 - Tabular
 - Event
 - TSSI
- Markers Add, Delete or G

🚔 list	
<u>File E</u> dit <u>V</u> iew <u>T</u> ool:	; <u>W</u> indow
ns-y delta-y	/testbench/stimulus_O/AEn-, /testbench/stimulus_O/CLK_JRise-, /te /testbench/stimulus_O/AFn-, /testbench/stimulus_O/CLK_MaxF /testbench/stimulus_O/CLK-, /testbench/stimulus_C /testbench/stimulus_O/CLK_Duty-, /testbench/s /testbench/stimulus_O/CLK_JFall-,
$\begin{array}{rrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrrr$	St0 St1 St1 50 0 0 St0 St1 St1 50 0 0
]	



Saving Tabular Output



Actel Corporation Confidential © 2009

636

Synplify Attributes and Directives

syn_keep *Directive*

- Maintains Net Throughout Synthesis
 - During Synthesis, Nets May Not Be Maintained in order to Create Optimized Circuit
- Applied to wires in Verilog and signals in VHDL
- Nets Can Be Preserved to
 - Probe their Values during Simulation
 - Prevent Certain Optimizations, such as Clock Enable Optimization

Example:

```
signal q_tmp : std_logic;
attribute syn_keep : boolean;
attribute syn_keep of q_tmp : signal is true;
```



alspreserve

Actel-Specific Attribute

- Keeps Net from Being Collapsed in Designer (Back-end) Tools
 - Must also Add **syn_keep** to Ensure Synplicity Retains Net
 - Synplicity Adds alspreserve Attribute to EDIF Netlist



alspreserve

Syntax

Verilog Syntax

```
object /* synthesis alspreserve = 1 */ ;
```

• Example:

module foo (in, out); input [6:0] in; output out; wire out; wire or_out1 /* synthesis syn_keep=1 alspreserve=1 */; wire and_out1; wire and_out2; wire and_out3 /* synthesis syn_keep=1 alspreserve=1 */;

VHDL Syntax

attribute also reserve of object : signal is true ;

• Example:

```
architecture comb of foo is
    signal and_out1, and_out2, and_out3, or_out1 : std_logic;
    attribute syn_keep of and_out3 : signal is true;
    attribute syn_keep of or_out1 : signal is true;
    attribute alspreserve: boolean;
    attribute alspreserve of and_out3 :signal is true;
    attribute alspreserve of or_out1 : signal is true;
```



syn_encoding

Attribute

- Sets Encoding Style for State Machines
 - Overrides Default Style
- Default Style Compiler Selects Encoding Style Based on Number of States as Follows:
 - 1 4 States: Sequential
 - 5 24 States: One-hot
 - > 24 States: Gray
- **syn_encoding** Can Have the Following Values:
 - onehot
 - gray
 - sequential
 - safe



syn_encoding

Attribute Usage

- SCOPE Constraint Editor Usage
 - Select Individual State Machines and Assign Attribute

ij sccwrap.sdc (constraint File) *							
	Object	Attribute	Value	Val Type	Description	Commei	
1	make_scc.UG02.make_TX.xmit_state[0:5]	syn_encoding	gray	string	FSM encoding (onehot, sequential, gray,		
2	make_scc.UG04.make_RX.rx_state[0:2]	syn_encoding	sequential	string	FSM encoding (onehot, sequential, gray,		
3							
4							
	Clocks 🔏 Clock to Clock 🔏 Inputs/Outputs	🔏 Registers 🔏 Multi-Cycle F	Paths 🔏 False Pati	hs 🔏 Max I	Delay Paths À Attributes Ă Oth ◀	•	



syn_encoding

Attribute Usage (cont.)

Verilog Syntax

```
object /* synthesis syn_encoding = "value" */ ;
```

• Example:

```
module prep3 (CLK, RST, IN, OUT);
input CLK, RST;
input [7:0] IN;
output [7:0] OUT;
reg [7:0] OUT;
reg [7:0] current_state /* synthesis syn_encoding="gray" */;
// Other code
```

VHDL Syntax

attribute syn_encoding of object : object_type is "string" ;

• Example:

```
library synplify;
use synplify.attributes.all;
package my_states is
type state is (st0, st1, st2, st3, st4, st5);
signal s1 : state;
attribute syn_encoding of s1 : signal is "gray";
end my_states;
```



syn_maxfan

Attribute

- Controls Maximum Fanout of Instance, Net, or Port
- Limit Specified by this Attribute May Be Treated as Hard or Soft Depending on Where It Was Specified
 - Soft Limit May Not Be Honored if it Degrades Performance
- You Can Apply syn_maxfan Attribute to Module, Register, Instance, Port, or Net
 - For ProASIC and APA Designs Only You Can also Apply to Module or Entity



syn_maxfan *Usage*

SCOPE Constraint Editor Usage

	C:/Actelprj/Actel_bootcamp/Sysmon_AFS_SOC_lab/Solutions/VHDL/SysMon/constraint/top_syn_1.sdc *								
	Enabled	Object Type	Object	Attribute	Value	Val Type	Description	Comment	
1	•	<any></any>	n:RESETn	syn_maxfan	10000	integer	Overrides the default fanout		
2									
3									Ŧ
Clo	icks Cl	ock to Clock Colle	ections Inputs/Outputs Registe	ers Delay Paths Attribute	I/O Standards	Compile	Points Other	<u>.</u>	_

SDC File Syntax

define_attribute { object } syn_maxfan { integer }

• Example – Limit Fanout for Signal clk to 200:





syn_maxfan Syntax

Verilog Syntax

```
object /* synthesis syn_maxfan = "value" */ ;
```

• Example:

```
module test (registered_data_out, clock, reset, data_in);
output [31:0] registered_data_out; input clock, reset;
input [31:0] data_in;
input reset /* synthesis syn_maxfan=1000 */;
// Other code
```

VHDL Syntax

attribute syn_maxfan of object: object_type is "value";

• Example:



syn_replicate Attribute

- Prevents Replication of Register
 - assign syn_replicate = 0 Turns Off Register Replication
 - Cannot Force Tool to Replicate
 - Works along with **max_fanout** Value
 - Only Supported on Individual Register
- When Will Synplify Replicate or Buffer?
 - Generally Flip-flops Are Replicated to Achieve Fan-out Control
 - Combinatorial Cells May be Replicated to Control Fanout


syn_replicate Usage

SCOPE Constraint Editor Usage

	iii find_min_syn.sdc (constraint File) *								
Object		Object	Attribute	Value	Val Type	_			
l	1	dstl1_n	syn_replicate	0					
	2	dstl2_n	syn_replicate	1		_			
l	×ÞK	Registers 🔏 Multi-Cycle Paths	🔏 False Paths 🔏 Max Delay Pa	aths∖∖Attr	ibutes /				

SDC File Syntax

define_global_attribute syn_replicate = { 1 | 0 }

Example - Disables All Replication in Design:

1 enables replication 0 disables replication

• • •
define_global_attribute syn_replicate {0}
• • •



syn_replicate Usage (cont.)

Verilog Syntax

```
0 disables replication
```

```
object /* synthesis syn_replicate = 1 | 0 */;
```

• Example:

```
module norep (Reset, Clk, Drive, OK, ADPad, IPad, ADOut);
    • •
.
reg [31:0] IPad;
reg DriveA /* synthesis syn_replicate = 0 */;
assign ADPad = DriveA ? ADOut : 32'bz;
always @(posedge Clk or negedge Reset)
        if (!Reset) begin
           DriveA <= 0;
           IPad <= 0; end
        else begin
           DriveA <= Drive & OK;
                  <= ADPad; end
           IPad
endmodule
```



syn_replicate Usage (cont.)

VHDL Syntax

false disables replication

- attribute syn_replicate of object : object_type is true | false ;
- Example:



syn_sharing Directive

- Enables/Disables Resource Sharing of Operators inside Module during Synthesis
 - By Default, Directive Is Enabled (Value 1 for Verilog, true for VHDL).
 - If Resource Sharing Check Box in Project View is Disabled, You Can Still Enable Resource Sharing Using syn_sharing Directive



syn_sharing Usage

- Verilog Syntax
 - object /* synthesis syn_sharing = 1 | 0 */;
 - Example:

```
module my_design(out,in,clk_in) /* synthesis syn_sharing=0 */;
```

// Other code

- VHDL Syntax
 - attribute syn_sharing of object : object_type is " true | false"; object can be architecture name
 - Example:



syn_noclockbuf

Synthesis Attribute

- Selects/Deselects Automatic Clock Buffering
 - Value of '1' (or Boolean TRUE) Turns OFF Automatic Clock Buffering
 - You Can Apply syn_noclockbuf Attribute to Module, Register, Instance, Port, or Net
- Synplicity SCOPE Constraint Editor Usage

C:/Actelprj/Actel_bootcamp/Sysmon_AFS_SOC_lab/Solutions/VHDL/SysMon/constraint/top_syn_1.sdc *							_0×		
	Enabled	Object Type	Object	Attribute	Value	Val Type	Description	Comment	
1	•	<any></any>	p:RESETn	syn_noclockbuf	0	boolean	Use normal input buffer		
2									
3									⊡
Clo	icks Cl	ock to Clock Colle	ections Inputs/Outputs Registe	ers Delay Paths Attribute	s I/O Standards	Compile	Points Other		



syn_noclockbuf

Attribute Usage (cont.)

- Verilog Syntax
 - object /* synthesis syn_noclockbuf = "value" */;
 - Example:

```
module test (registered_data_out, clock, reset, data_in);
output [31:0] registered_data_out; input clock;
input [31:0] data_in;
input reset /* synthesis syn_noclockbuf=1 */;
// Other code
```

VHDL Syntax

- attribute syn_noclockbuf of object : object_type is "value" ;
- Example:



syn_global_buffers

Synthesis Attribute (ProASIC3/E, Fusion, IGLOO/e)

Specifies The Number Of Global Buffers To Be Used

- Use This Attribute To Restrict The Number Of Global Buffer Resources Used by Synplicity
- Attribute Is Applied Globally On The Top-level Module Or Entity
- Value Can Be Any Integer Between 6 And 18
- Synplicity SCOPE Constraint Editor Usage

	C:/Actelprj/Actel_bootcamp/Cortex-M1_AFS_SOC_lab/Solutions/VHDL/M1AFS_SOC/constraint/SOC_TOP_syn.sdc *								
		Enabled	Object Type	Object	Attribute	Value	Val Type	Description	Comment
	1	•	global	<global></global>	syn_global_buffers	8	integer	Number of global buffers	
	2								
	3								▲ ▼
ĺ	Clo	icks Cl	ock to Clock Colle	ections Inputs/Outputs Registe	ers Delay Paths Attribute	s I/O Standards	Compile	Points Other	



syn_global_buffers

Attribute Usage

Verilog Syntax

object /* synthesis syn_global_buffers = <maximum> */;

• Example:

```
module top (clk1, clk2, clk3, clk4, clk5, clk6,
clk7,clk8,clk9, clk10, clk11, clk12, clk13, clk14, clk15,
d1, d2, d3, d4, d5, q1, q2, reset)
/* synthesis syn_global_buffers = 10 */;
```

VHDL Syntax

attribute syn_global_buffers of object : object_type is
 <maximum>;

• Example:

```
entity top is
   port( ... );
end top;
architecture behave of top is
attribute syn_global_buffers : integer;
attribute syn_global_buffers of behave : architecture is 10;
```



syn_ramstyle

Synthesis Attribute

- Manually Indicates How Inferred RAM is Implemented
- Values
 - block_ram (default) Inferred RAM Will Use Block RAM if Possible
 - RAM Larger than One Block Will Be Cascaded
 - By Default, Software Uses Deep Block RAM Configurations instead of Wide Configurations for Better Timing Results
 - Example: 4Kx8 Built from 512x8s instead of 4Kx1s
 - Deeper RAMS Reduces Output Data Delay Timing by Reducing the MUX Logic at RAM Outputs of the RAMS
 - registers Inferred RAM Will Be Implemented as Registers
 - **no_rw_check** Implements RAM without Glue Logic
 - Glue Logic to Bypass RAM Is Added by Default because Simultaneous Read and Write at the Same Address Gives Indeterminate Data
 - Possible Simulation Mismatch
- syn_ramstyle Attribute Is Applied to Memory Array
- Value of select_ram (Indicated in Documentation) Does Not Apply to Actel RAMs

