

Advanced Training Course on FPGA Design and VHDL for Hardware  
Simulation and Synthesis | (smr 2065)

Contribution ID : 35

Type : **not specified**

## Laboratory Session. Synthesis and Post-Synthesis Simulation (cont.)

*Tuesday, 3 November 2009 16:00 (2:00)*

**Content**

**Summary**

**Primary author(s) :** M.L. CRESPO

**Presenter(s) :** M.L. CRESPO

**Session Classification :** Laboratory Session. Synthesis and Post-Synthesis Simulation (cont.)