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ICTP Latin-American Basic Course on FPGA Design for Scientific Instrumentation | (smr 2177)

Monday 15 March 2010

REGISTRATION AND ADMINISTRATIVE FORMALITIES - - Room alternative: LOBBY, UCAECE UNIVERSITY MAIN ENTRANCE (09:00-11:30)

time	title	presenter
09:00	REGISTRATION AND ADMINISTRATIVE FORMALITIES	

OPENING CEREMONY - - Room alternative: AULA MAGNA CAECE UNIVERSITY (11:30-13:00)

time	title	presenter
11:30	OPENING CEREMONY	

Lunch (13:00-14:00)

time	title	presenter
13:00	Lunch	

FPGA Design and VHDL. Overview. (14:00-15:00)

time	title	presenter
14:00	FPGA Design and VHDL. Overview.	NIZAR ABDALLAH

Coffee break (15:00-15:30)

time	title	presenter
15:00	Coffee break	

FPGA Architectures & VHDL. Introduction to FPGAs & FPGA Design Flow. (15:30-16:30)

time	title	presenter
15:30	FPGA Architectures & VHDL. Introduction to FPGAs & FPGA Design Flow.	NIZAR ABDALLAH

Introduction to Digital Design. (16:30-17:30)

time	title	presenter
16:30	Introduction to Digital Design.	PIROUZ BAZARGAN-SABET

Digital Design I (combinatorial elements). (17:30-18:30)

time	title	presenter
17:30	Digital Design I (combinatorial elements).	PIROUZ BAZARGAN-SABET

Tuesday 16 March 2010

Digital Design II (sequential elements, Mealy and Moore FSM). (09:00-10:00)

time	title	presenter
09:00	Digital Design II (sequential elements, Mealy and Moore FSM).	PIROUZ BAZARGAN-SABET

FPGA Architectures & VHDL. Introduction to Synthesis. (10:00-11:00)

time	title	presenter
10:00	FPGA Architectures & VHDL. Introduction to Synthesis.	NIZAR ABDALLAH

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Synthesis II - Introduction to VHDL. (11:30-12:30)

time	title	presenter
11:30	Synthesis II - Introduction to VHDL.	NIZAR ABDALLAH

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

(LiberoTM IDE) Design Entry. (14:00-15:00)

time	title	presenter
14:00	(LiberoTM IDE) Design Entry.	NIZAR ABDALLAH

Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc). (15:00-16:00)

time	title	presenter
15:00	Digital Design III (more complex elements: RAM, ROM, buses, pipeline concept, etc).	PIROUZ BAZARGAN-SABET

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

(LiberoTM IDE) Functional Simulation. Synthesis. (16:30-17:30)

time	title	presenter
16:30	(LiberoTM IDE) Functional Simulation. Synthesis.	NIZAR ABDALLAH

Synthesis III - Advanced VHDL. (17:30-18:30)

time	title	presenter
17:30	Synthesis III - Advanced VHDL.	NIZAR ABDALLAH

Wednesday 17 March 2010

Digital arithmetic I (number representations). (09:00-10:00)

time	title	presenter
09:00	Digital arithmetic I (number representations).	PIROUZ BAZARGAN-SABET

(LiberoTM IDE) Place & Route. (10:00-11:00)

time	title	presenter
10:00	(LiberoTM IDE) Place & Route.	NIZAR ABDALLAH

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Design Verification and Timing Concepts. (11:30-12:30)

time	title	presenter
11:30	Design Verification and Timing Concepts.	NIZAR ABDALLAH

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

(LiberoTM IDE) Timing Constraints and Analysis (14:00-15:00)

time	title	presenter
14:00	(LiberoTM IDE) Timing Constraints and Analysis	NIZAR ABDALLAH

Digital arithmetic II (basic arithmetic operations). (15:00-16:00)

time	title	presenter
15:00	Digital arithmetic II (basic arithmetic operations).	PIROUZ BAZARGAN-SABET

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Programmable logic & FPGA architectures (16:30-17:30)

time	title	presenter
16:30	Programmable logic & FPGA architectures	NIZAR ABDALLAH

(LiberoTM IDE) Post-Layout Simulation. FPGA Programming. (17:30-18:30)

time	title	presenter
17:30	(LiberoTM IDE) Post-Layout Simulation. FPGA Programming.	NIZAR ABDALLAH

Thursday 18 March 2010

Actel Fusion FPGA architecture. (09:00-10:00)

time	title	presenter
09:00	Actel Fusion FPGA architecture.	NIZAR ABDALLAH

Actel Fusion FPGA architecture (cont.) (10:00-11:00)

time	title	presenter
10:00	Actel Fusion FPGA architecture (cont.)	NIZAR ABDALLAH

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

The Actel Fusion Embedded Development Kit (11:30-12:30)

time	title	presenter
11:30	The Actel Fusion Embedded Development Kit	NIZAR ABDALLAH

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

The Actel Fusion Embedded Development Kit (cont.) (14:00-15:00)

time	title	presenter
14:00	The Actel Fusion Embedded Development Kit (cont.)	NIZAR ABDALLAH

Laboratory Overview. VHDL Simulation Environment. A design example. (15:00-16:00)

time	title	presenter
15:00	Laboratory Overview. VHDL Simulation Environment. A design example.	MARIA LIZ CRESPO

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Laboratory Exercises: VHDL Behavioral Description and Simulation of Combinational Circuits. (16:30-18:30)

time	title	presenter
16:30	Laboratory Exercises: VHDL Behavioral Description and Simulation of Combinational Circuits.	

Friday 19 March 2010

System-on-Chip concepts (09:00-10:00)

time	title	presenter
09:00	System-on-Chip concepts	NIZAR ABDALLAH

System-on-Chip concepts (cont.) (10:00-11:00)

time	title	presenter
10:00	System-on-Chip concepts (cont.)	NIZAR ABDALLAH

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Laboratory Exercises: VHDL Behavioral Description and Simulation of Combinational Circuits (cont.) (11:30-12:30)

time	title	presenter
11:30	Laboratory Exercises: VHDL Behavioral Description and Simulation of Combinational Circuits (cont.)	

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

Laboratory Exercises: VHDL Behavioral Description and Simulation of Combinational Circuits (cont.) (14:00-15:00)

time	title	presenter
14:00	Laboratory Exercises: VHDL Behavioral Description and Simulation of Combinational Circuits (cont.)	

Basic Add and Subtract Operations in VHDL. Case examples. (15:00-16:00)

time	title	presenter
15:00	Basic Add and Subtract Operations in VHDL. Case examples.	CRISTIAN SISTERNA

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Laboratory Exercises: VHDL Behavioral Description and Simulation of Sequential Circuits (16:30-18:30)

time	title	presenter
16:30	Laboratory Exercises: VHDL Behavioral Description and Simulation of Sequential Circuits	

Monday 22 March 2010

Microelectronics at CERN (09:00-10:00)

time	title	presenter
09:00	Microelectronics at CERN	PAULO RODRIGUES S. MOREIRA

Introduction to CMOS Technology and VLSI Design. (10:00-11:00)

time	title	presenter
10:00	Introduction to CMOS Technology and VLSI Design.	PAULO RODRIGUES S. MOREIRA

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

CMOS Technology I (11:30-12:30)

time	title	presenter
11:30	CMOS Technology I	PAULO RODRIGUES S. MOREIRA

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

Laboratory Exercises: VHDL Behavioral Description and Simulation of Sequential Circuits (cont.) (14:00-16:00)

time	title	presenter
14:00	Laboratory Exercises: VHDL Behavioral Description and Simulation of Sequential Circuits (cont.)	

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Laboratory Exercises: Finite State Machine. VHDL Description and Simulation. (16:30-18:30)

time	title	presenter
16:30	Laboratory Exercises: Finite State Machine. VHDL Description and Simulation.	

Tuesday 23 March 2010

Introduction to Fourier Theory. (09:00-10:00)

time	title	presenter
09:00	Introduction to Fourier Theory.	MARCELO MAGNASCO

Fourier Theory I. (10:30-11:30)

time	title	presenter
10:30	Fourier Theory I.	MARCELO MAGNASCO

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

CMOS Technology II. (11:30-12:30)

time	title	presenter
11:30	CMOS Technology II.	PAULO RODRIGUES S. MOREIRA

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

VLSI Design. (14:00-15:00)

time	title	presenter
14:00	VLSI Design.	PAULO RODRIGUES S. MOREIRA

Laboratory Exercises: Finite State Machine. VHDL Description and Simulation (cont.) (15:00-16:00)

time	title	presenter
15:00	Laboratory Exercises: Finite State Machine. VHDL Description and Simulation (cont.)	

Coffee break (16:00-16:30)

time	title	presenter

16:00	Coffee break	

Laboratory Exercises: Finite State Machine. Synthesis and Post-Synthesis Simulation. (16:30-18:30)

time	title	presenter
16:30	Laboratory Exercises: Finite State Machine. Synthesis and Post-Synthesis Simulation.	

Wednesday 24 March 2010

Fourier Theory II. (09:00-10:00)

time	title	presenter
09:00	Fourier Theory II.	MARCELO MAGNASCO

Introduction to Digital Signal Processing. (10:00-11:00)

time	title	presenter
10:00	Introduction to Digital Signal Processing.	MARCELO MAGNASCO

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Advanced FPGA Applications. (11:30-12:30)

time	title	presenter
11:30	Advanced FPGA Applications.	ALEXANDER KLUGE

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

A case study in HEP experiments I. (14:00-15:00)

time	title	presenter
14:00	A case study in HEP experiments I.	ALEXANDER KLUGE

Laboratory Exercises: Finite State Machine. Synthesis and Post-Synthesis Simulation (cont.) (15:00-16:00)

time	title	presenter
15:00	Laboratory Exercises: Finite State Machine. Synthesis and Post-Synthesis Simulation (cont.)	

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Hardware Description of the FPGA Development Platform. (16:30-17:30)

time	title	presenter
16:30	Hardware Description of the FPGA Development Platform.	CARLOS SOSA PAEZ

FPGA Implementation Example. (17:30-18:30)

time	title	presenter
17:30	FPGA Implementation Example.	CRISTIAN SISTERNA

Thursday 25 March 2010

Digital Signal Processing I (09:00-10:00)

time	title	presenter
09:00	Digital Signal Processing I	MARCELO MAGNASCO

Digital Signal Processing II (10:00-11:00)

time	title	presenter
10:00	Digital Signal Processing II	MARCELO MAGNASCO

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

A case study in HEP experiments II (11:30-12:30)

time	title	presenter
11:30	A case study in HEP experiments II	ALEXANDER KLUGE

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

A case study in HEP experiments III (14:00-15:00)

time	title	presenter
14:00	A case study in HEP experiments III	ALEXANDER KLUGE

Laboratory Exercises: Implementation in the FPGA Development Platform. (15:00-16:00)

time	title	presenter
15:00	Laboratory Exercises: Implementation in the FPGA Development Platform.	

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Laboratory Exercises: Implementation in the FPGA Development Platform (contd.) (16:30-18:30)

time	title	presenter
16:30	Laboratory Exercises: Implementation in the FPGA Development Platform (contd.)	

Friday 26 March 2010

Selected topics on Logic Synthesis and FPGA Debugging. (09:00-10:00)

time	title	presenter
09:00	Selected topics on Logic Synthesis and FPGA Debugging.	ANDRES CICUTTIN

Selected topics on Logic Synthesis and FPGA Debugging (cont.) (10:00-11:00)

time	title	presenter
10:00	Selected topics on Logic Synthesis and FPGA Debugging (cont.)	ANDRES CICUTTIN

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Reconfigurable Virtual Instrumentation (RVI) based on FPGA. (11:30-12:30)

time	title	presenter
11:30	Reconfigurable Virtual Instrumentation (RVI) based on FPGA.	ANDRES CICUTTIN

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

Reconfigurable Virtual Instrumentation (RVI) based on FPGA (cont.) (14:00-15:00)

time	title	presenter
14:00	Reconfigurable Virtual Instrumentation (RVI) based on FPGA (cont.)	ANDRES CICUTTIN

The µLab Virtual Panel. A design example. (15:00-16:00)

time	title	presenter
15:00	The µLab Virtual Panel. A design example.	MIGUEL RISCO CASTILLO

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

The µLab Virtual Panel. A design example. (contd). (16:30-17:30)

time	title	presenter
16:30	The µLab Virtual Panel. A design example. (contd).	

Laboratory Exercises: Implementation in the FPGA Development Platform (cont.) (17:30-18:30)

time	title	presenter
17:30	Laboratory Exercises: Implementation in the FPGA Development Platform (cont.)	

Monday 29 March 2010

Radiation Effects in Semiconductor Devices. (09:00-10:00)

time	title	presenter
09:00	Radiation Effects in Semiconductor Devices.	FELIX PALUMBO

Radiation Effects in Semiconductor Devices. (10:00-11:00)

time	title	presenter
10:00	Radiation Effects in Semiconductor Devices.	FELIX PALUMBO

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Advanced Data Acquisition and Processing System for a HEP Experiment at CERN (11:30-12:30)

time	title	presenter
11:30	Advanced Data Acquisition and Processing System for a HEP Experiment at CERN	MARIA LIZ CRESPO

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

Laboratory Exercises: Digital Arithmetic. (14:00-16:00)

time	title	presenter
14:00	Laboratory Exercises: Digital Arithmetic.	

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Laboratory Exercises: Waveform generation (16:30-18:30)

time	title	presenter
16:30	Laboratory Exercises: Waveform generation	

Tuesday 30 March 2010

ICTP RVI Platform Description. (09:00-10:00)

time	title	presenter
09:00	ICTP RVI Platform Description.	ANDRES AIRABELLA

DEMO: ICTP RVI Platform. Virtual Instruments: Waveform Generator and Digital Oscilloscope (10:00-11:00)

time	title	presenter
10:00	DEMO: ICTP RVI Platform. Virtual Instruments: Waveform Generator and Digital Oscilloscope	MIGUEL RISCO CASTILLO

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Digital Signal Processing with FPGA. A Design Example: Differentiator. (11:30-12:30)

time	title	presenter
11:30	Digital Signal Processing with FPGA. A Design Example: Differentiator.	CARLOS SOSA PAEZ

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

Digital Signal Processing with FPGA. A Design Example: Differentiator (cont.) (14:00-15:00)

time	title	presenter
14:00	Digital Signal Processing with FPGA. A Design Example: Differentiator (cont.)	CARLOS SOSA PAEZ

Laboratory Exercises: Digital Signal Processing with FPGA. (15:00-16:00)

time	title	presenter
15:00	Laboratory Exercises: Digital Signal Processing with FPGA.	

Coffee break (16:00-16:30)

time	title	presenter
16:00	Coffee break	

Laboratory Exercises: Digital Signal Processing with FPGA. (contd.) (16:30-18:30)

time	title	presenter
16:30	Laboratory Exercises: Digital Signal Processing with FPGA. (contd.)	

Wednesday 31 March 2010

Laboratory Exercises: Digital Signal Processing with FPGA. (09:00-10:00)

time	title	presenter
09:00	Laboratory Exercises: Digital Signal Processing with FPGA.	

Digital Signal Processing with FPGA. A Design Example using the µLab Virtual Panel (constant multiplier and level shifter). (10:00-11:00)

time	title	presenter
10:00	Digital Signal Processing with FPGA. A Design Example using the µLab Virtual Panel (constant multiplier and level shifter).	ANDRES AIRABELLA

Coffee break (11:00-11:30)

time	title	presenter
11:00	Coffee break	

Digital Signal Processing with FPGA. A Design Example using the µLab Virtual Panel (constant multiplier and level shifter) (contd). (11:30-12:30)

time	title	presenter
11:30	Digital Signal Processing with FPGA. A Design Example using the µLab Virtual Panel (constant multiplier and level shifter) (contd).	

Lunch (12:30-14:00)

time	title	presenter
12:30	Lunch	

General Discussions and Concluding Remarks (14:00-15:00)

time	title	presenter
14:00	General Discussions and Concluding Remarks	

Coffee break (15:00-15:30)

time	title	presenter
15:00	Coffee break	

Distribution of Diplomas of Attendance (15:30-16:30)

time	title	presenter
15:30	Distribution of Diplomas of Attendance	

Get-Together Drink (16:30-18:30)

time	title	presenter
16:30	Get-Together Drink	