





Outline

Digital CMOS design

-  Boolean algebra
-  Basic digital CMOS gates
-  Combinational and sequential circuits
-  Coding - Representation of numbers

Basic CMOS Gates

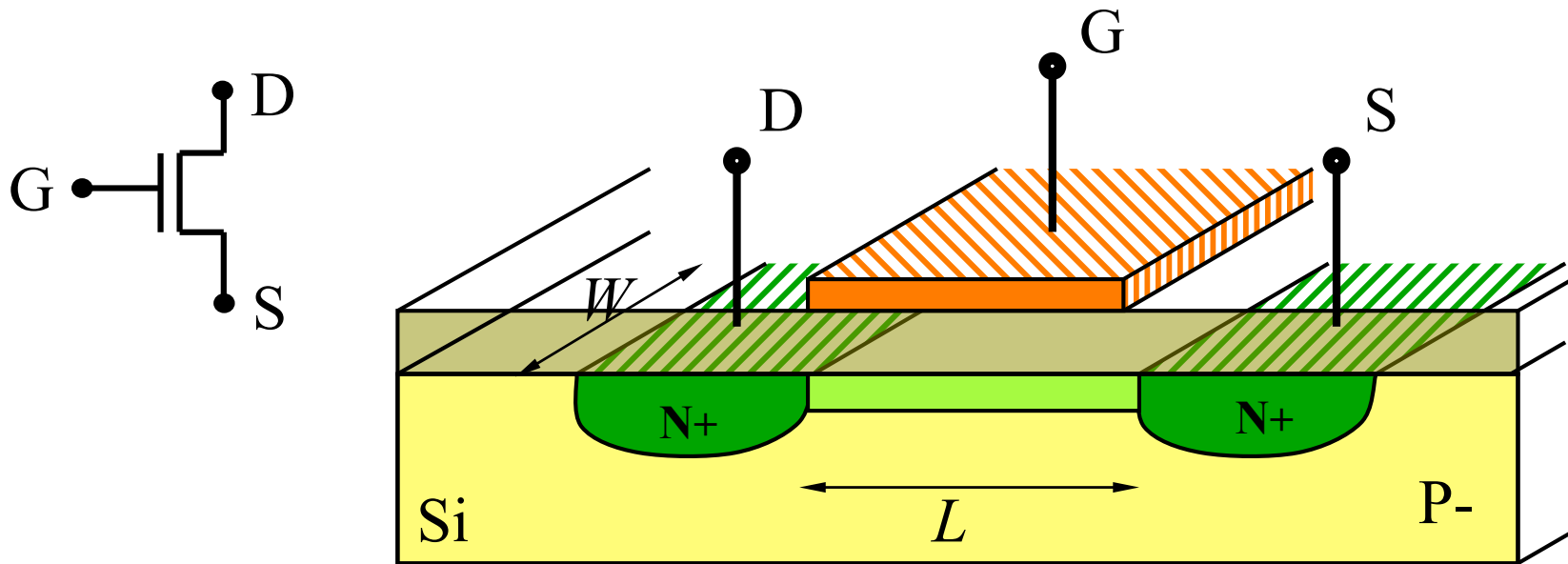
How to implement Boolean functions
in CMOS technology ?

Which functionalities are available



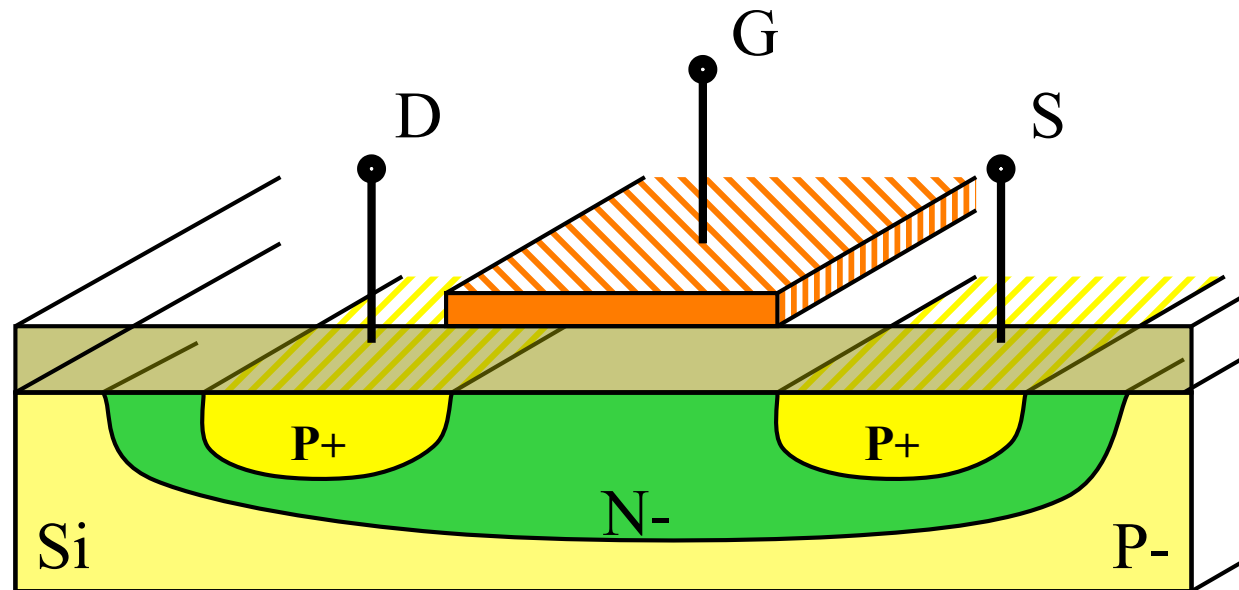
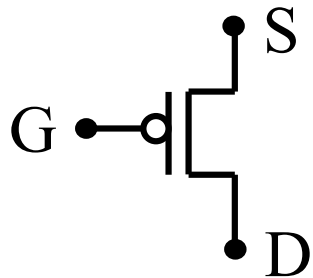
Basic CMOS Gates

● N-MOS transistor



Basic CMOS Gates

● P-MOS transistor



Basic CMOS Gates

The electrical behavior of a MOS transistor
is very complex

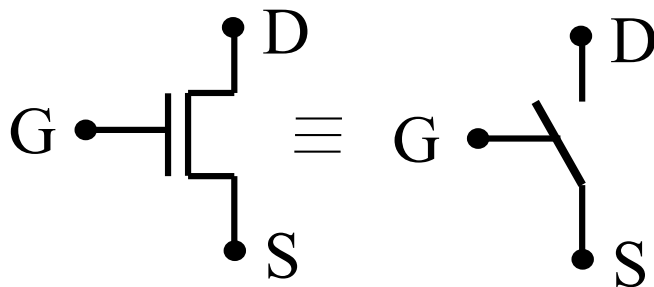
Design of a multi-million transistor circuit ?



Basic CMOS Gates

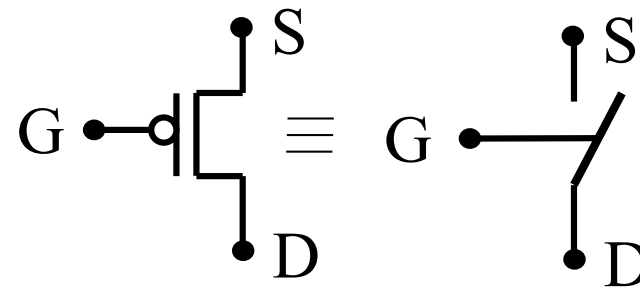
In a digital circuit a MOS transistor can be
seen as a **Switch**

N-MOS



$D = S$ when $G = 1$

P-MOS



$D = S$ when $G = 0$

Basic CMOS Gates

When driving, a MOS transistor can be seen as a **Resistor**

$$\text{Conductance} \propto \frac{W}{L}$$

For the same size, a P-MOS is twice
more resistive than an N-MOS



Basic CMOS Gates

The N-MOS and P-MOS are not exactly symmetrical

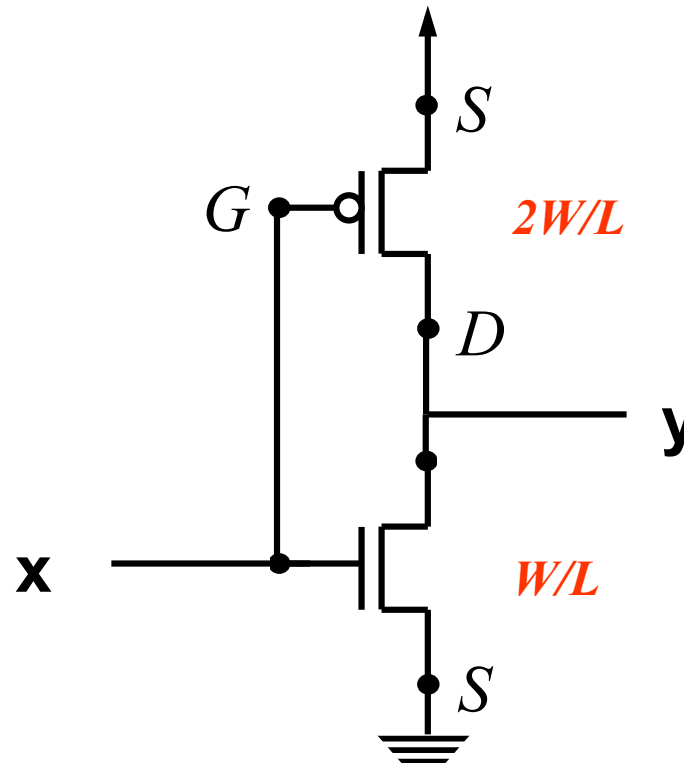
A N-MOS is a good transmitter of 0

A P-MOS is a good transmitter of 1

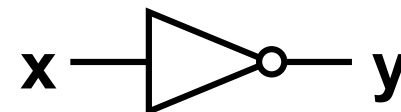


Basic CMOS Gates

$$y = \text{Not } x$$

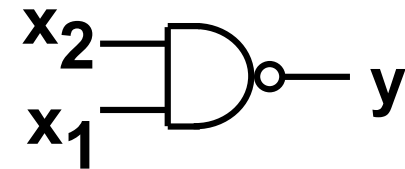
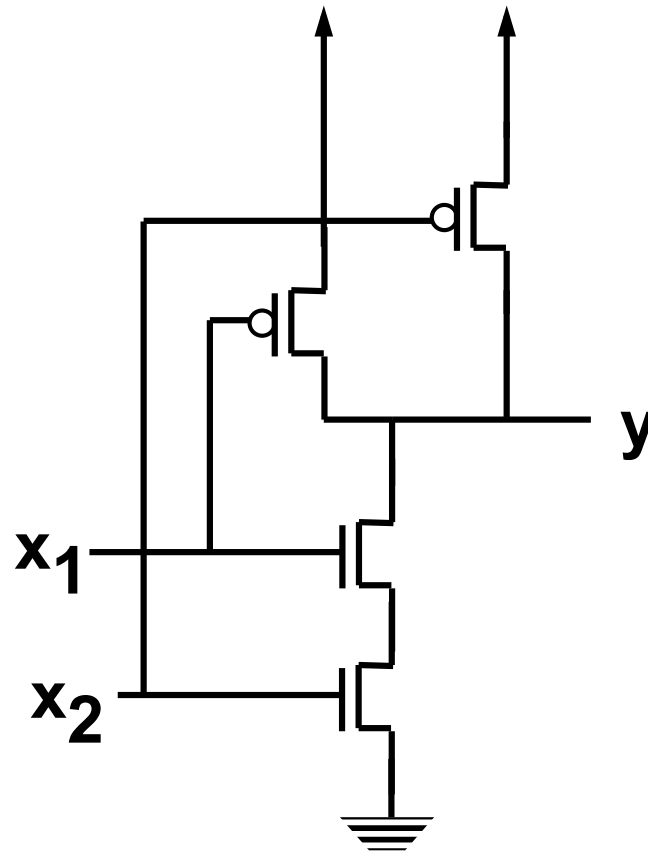


Dual CMOS gate



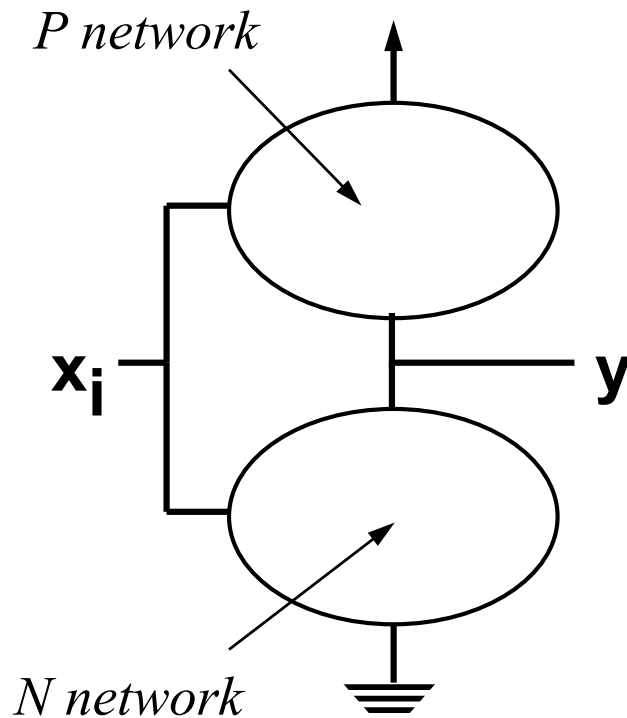
Basic CMOS Gates

$$y = \overline{x_1 \cdot x_2}$$



Basic CMOS Gates

Design of a dual gate



The P-network must be the dual of the N-network

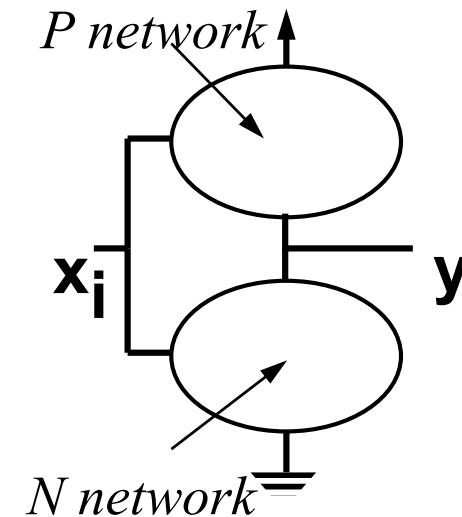
Series \longrightarrow Parallel
Parallel \longrightarrow Series

Take care of the size of transistors

Basic CMOS Gates

- To set the output to **0** a path has to be created through the **N** network
- A series of N-transistor must be conducting

$$\prod x_i = 1$$



Only negative (inverting) functions can be created

Basic CMOS Gates

Implementing a Boolean function with a CMOS gate ?

- The function must be inverting in regard of all the variables
- Put the function in the form of $f = \overline{g}$
- Design the N-network of g

Basic CMOS Gates

Implementing a Boolean function with a CMOS gate ?

- In the expression of **g** each ' **\cdot** ' are two paths in series
- In the expression of **g** each ' **$+$** ' are two paths in parallel
- The P-network is the dual network of the N-network
- **Avoid putting more than 3 transistors in series**



Basic CMOS Gates

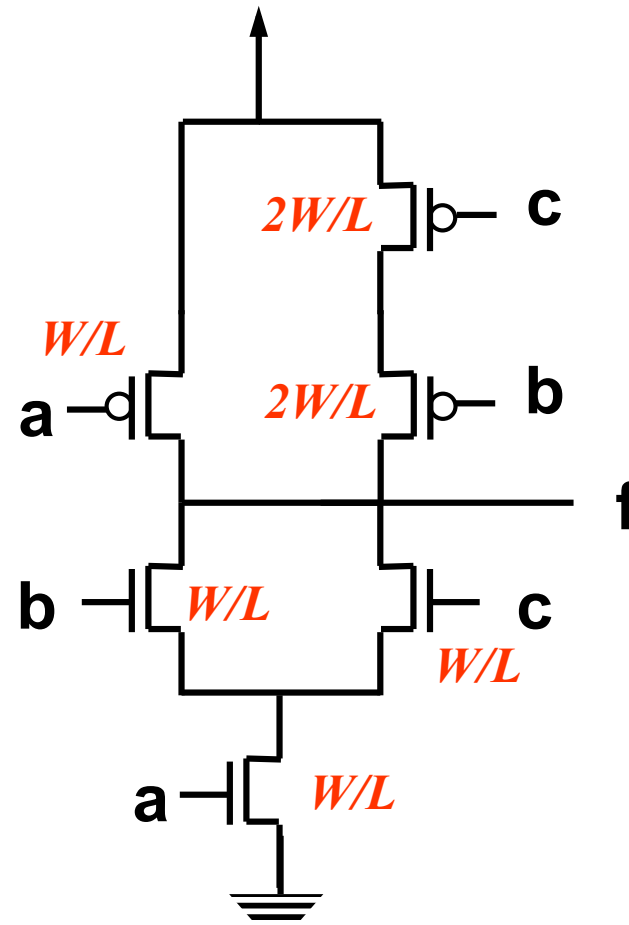
Example :

$$f = \bar{a} + (\bar{b} \cdot \bar{c})$$

$$f = \bar{a} + \overline{(b+c)}$$

$$f = \overline{a \cdot (b+c)}$$

$$g = a \cdot (b+c)$$



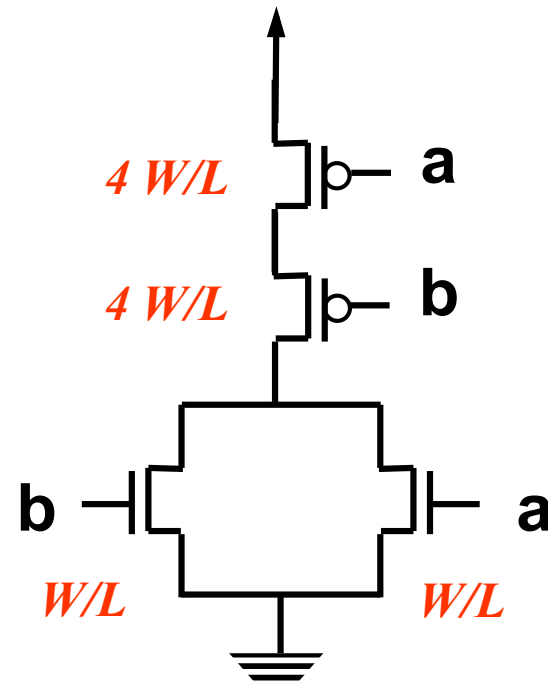
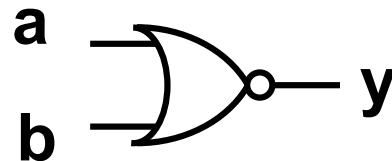
Basic CMOS Gates

Some gates :

Inverter : $f = \overline{a}$

Nand : $f = \overline{a.b}$

Nor : $f = \overline{a+b}$

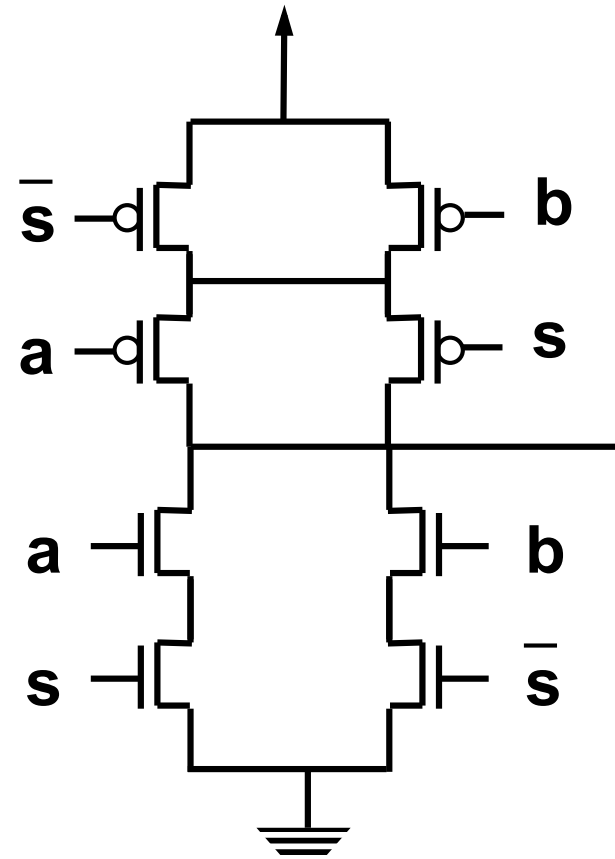
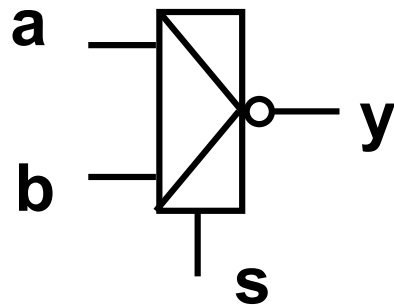


Basic CMOS Gates

Some gates :

Multiplexer :

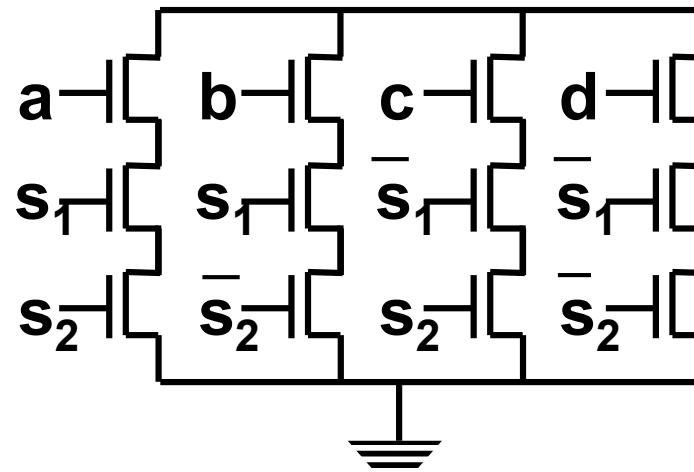
$$f = a.s + \bar{b}.s$$



Basic CMOS Gates

Some gates : Multiplexer :

$$f = a.s_1.s_2 + b.\bar{s}_1.s_2 + c.s_1.\bar{s}_2 + d.s_1.\bar{s}_2$$

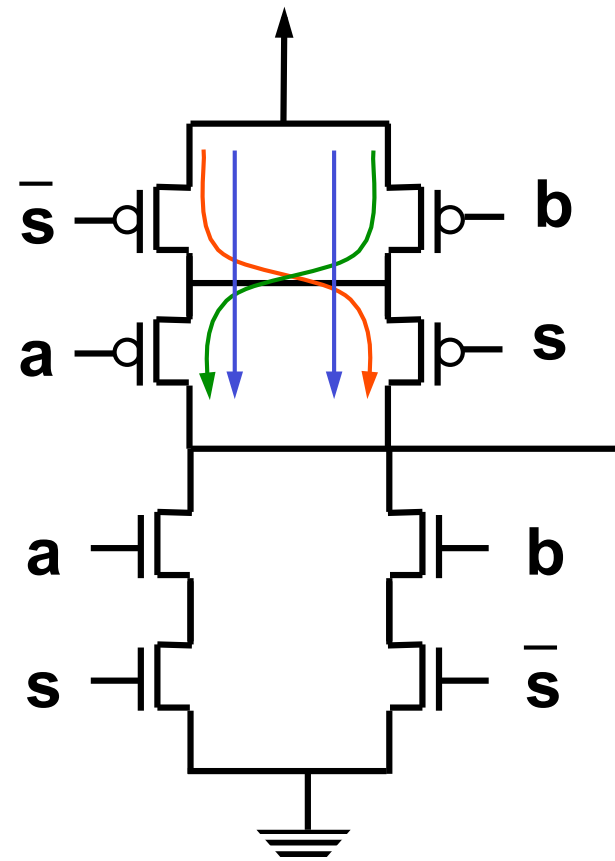


Basic CMOS Gates

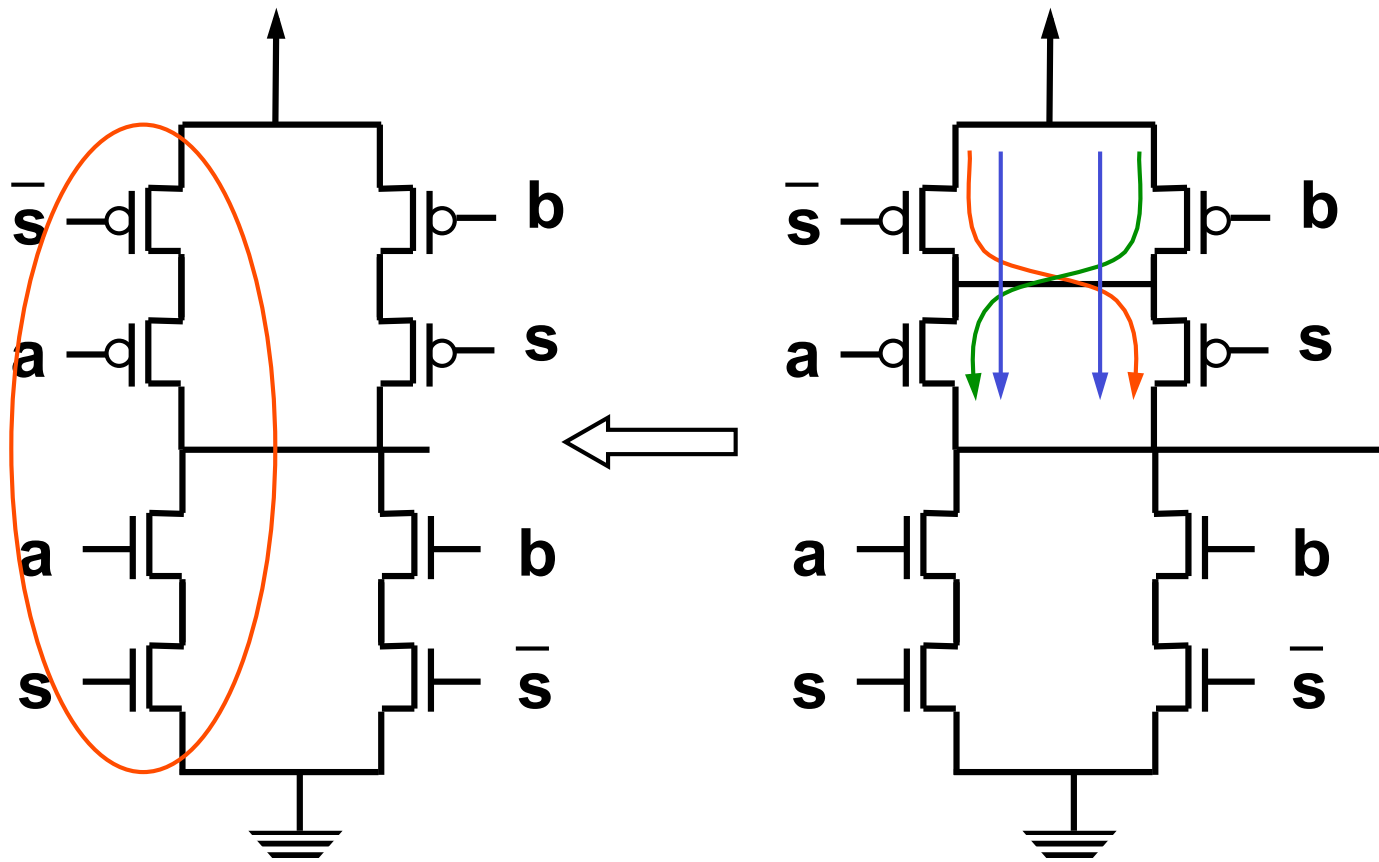
Some gates :

Multiplexer :

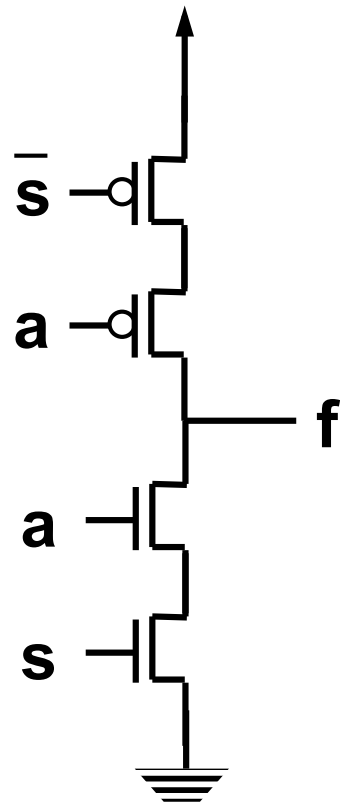
$$f = a.s + \bar{b}.s$$



Basic CMOS Gates

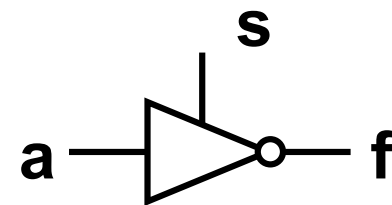


Basic CMOS Gates



If $s = 1$
 $f = \bar{a}$

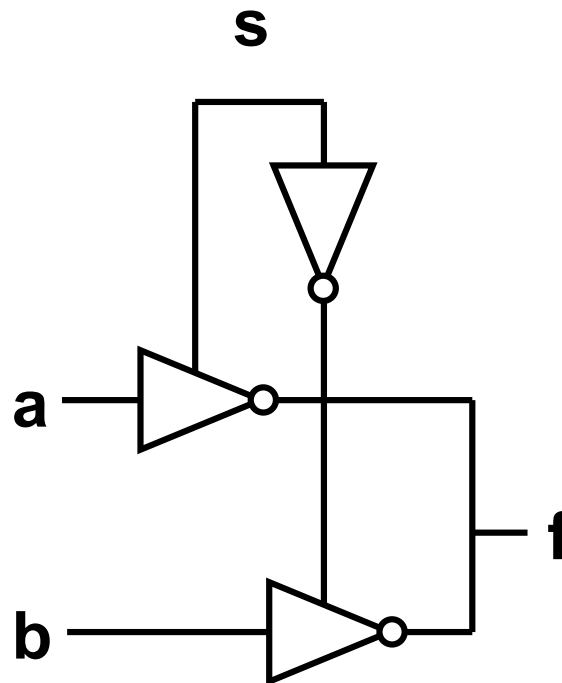
If $s = 0$
 f is not defined



Tri-state driver

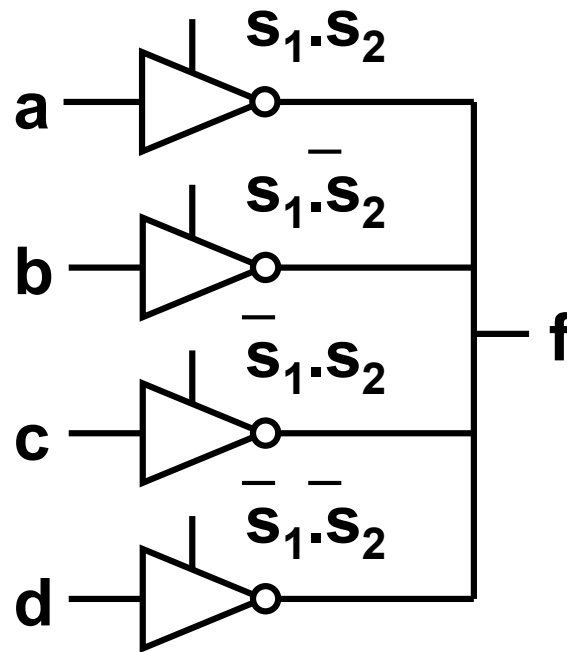
Basic CMOS Gates

Some gates : Multiplexer :



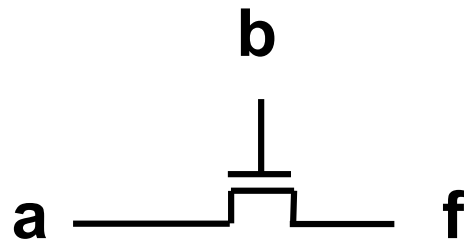
Basic CMOS Gates

Some gates : Multiplexer :



Basic CMOS Gates

Some gates :



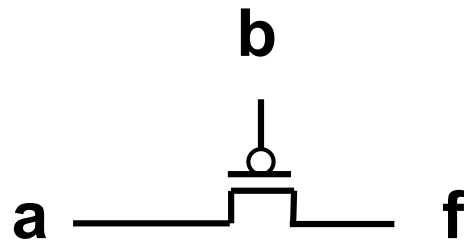
If **b = 1** If **b = 0**
f = a **f** is not defined

→ If **a = 0** then **f = 0**
→ If **a = 1** then **f = 1**

Pass-transistor

Basic CMOS Gates

Some gates :



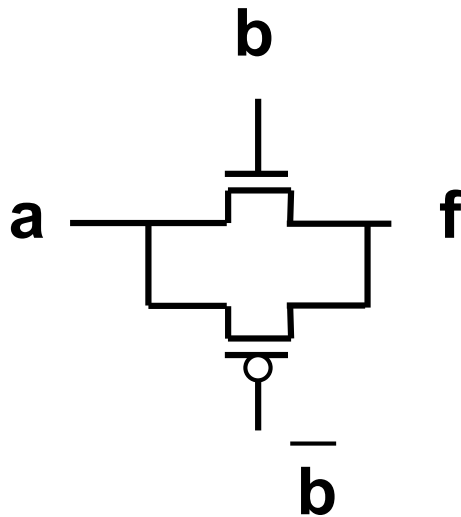
If **b** = 0 If **b** = 1
f = **a** **f** is not defined

- If **a** = 1 then **f** = 1
- If **a** = 0 then **f** = **0⁺**

Pass-transistor

Basic CMOS Gates

Some gates :



If **b = 1** If **b = 0**
f = a **f** is not defined

→ If **a = 0** then **f = 0**
→ If **a = 1** then **f = 1**

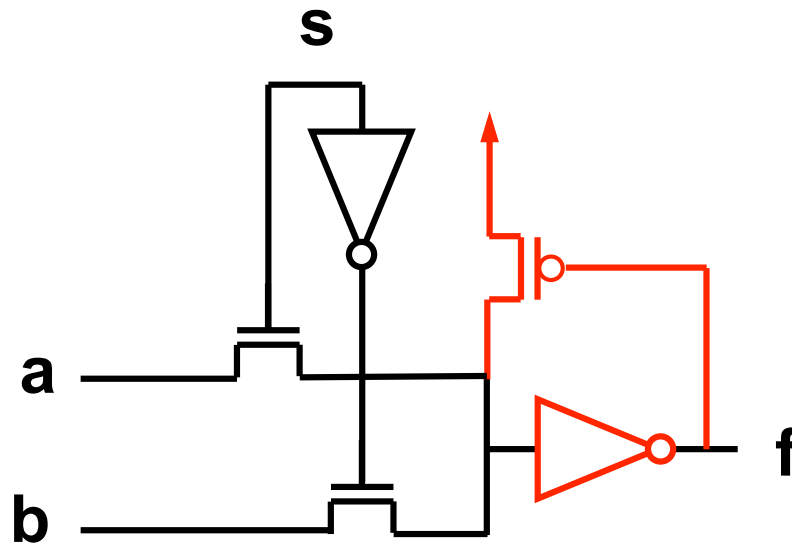
CMOS Switch

Basic CMOS Gates

Some gates :

Multiplexer :

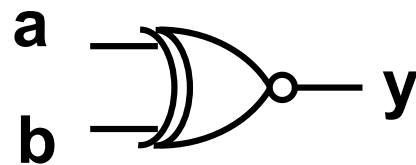
$$f = \overline{a.s} + \overline{b.s}$$



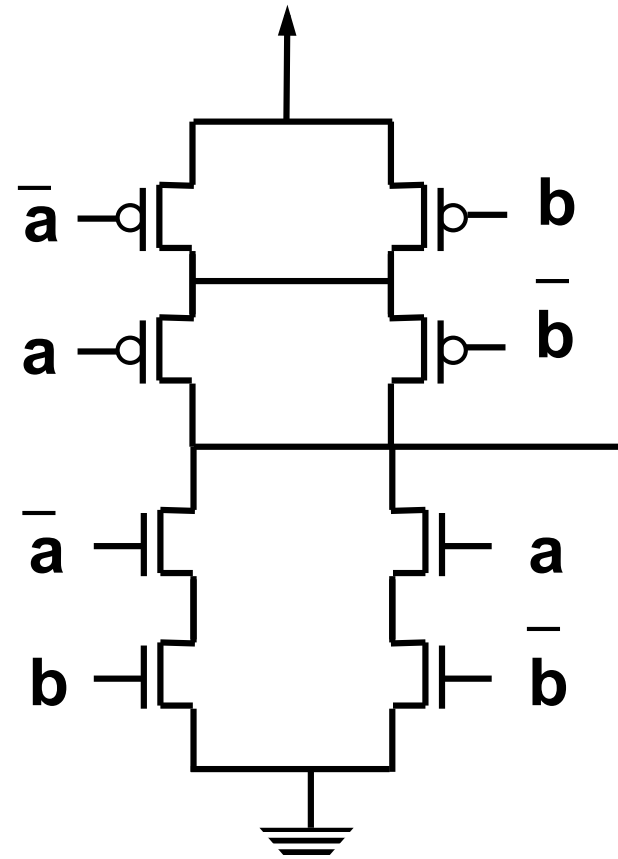
Basic CMOS Gates

Some gates :

$$\text{Nxor} : f = \overline{\overline{a}.b + a.\overline{b}}$$



I need \overline{a} and \overline{b}



Basic CMOS Gates

Some gates :

Xor with Pass-transistors :

$$f = \overline{a.b} + a.\overline{b}$$

a	b	f
0	0	1
0	1	0
1	0	0
1	1	1

