2384-10

ICTP Latin-American Advanced Course on FPGADesign for Scientific Instrumentation

19 November - 7 December, 2012

FPGA Introduction

SISTERNA Cristian Alejandro

Universidad Nacional de San Juan
Instituto de Investigaciones Antisismicas
Av. San Martin 1290 - Oeste
5400 San Juan
ARGENTINA

FPGA INTRODUCTION

Cristian AlejandroSisterna, MSc
Universidad Nacional San Juan
Argentina

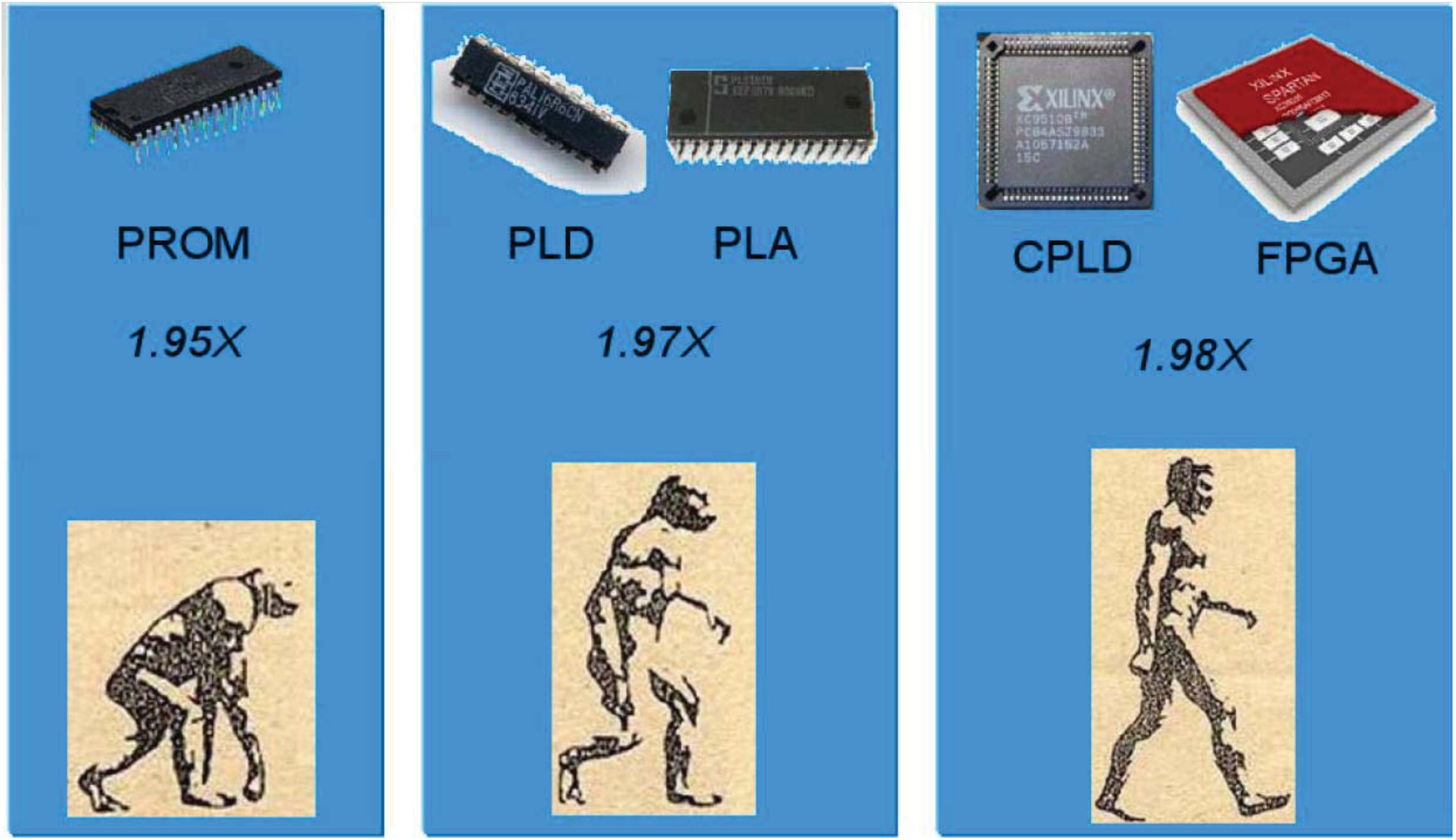
ICTP 2012 - CUBA

Agenda

- Introduction
- FPGA Architecture
- Configuration and routing cells
- Basic slice resources available in Xilinx FPGAs
- Basic I/O resources available in Xilinx FPGAs
- Clocking resources
- Memory blocks and distributed memory
- Multipliers and DSP blocks
- Routing
- Spartan 6, Virtex 6, Virtex 7
- FPGA Configuration

Introduction

PLDs Evolution



FPGA?

- Field
- Programmable
- Gate
- Array

FPGA: Competitive Market

FPGA
~~2000~~
2012

Altera Inc.	Actel Corp.
~~Lucent Technology~~	~~Philips Semiconductors~~
~~Intel Corp.~~	~~Motorola Semiconductors~~
~~QuickLogic~~	~~Cypress~~
Lattice Semiconductors	~~AMD~~
~~Vantis~~	Xilinx

FPGA Architecture

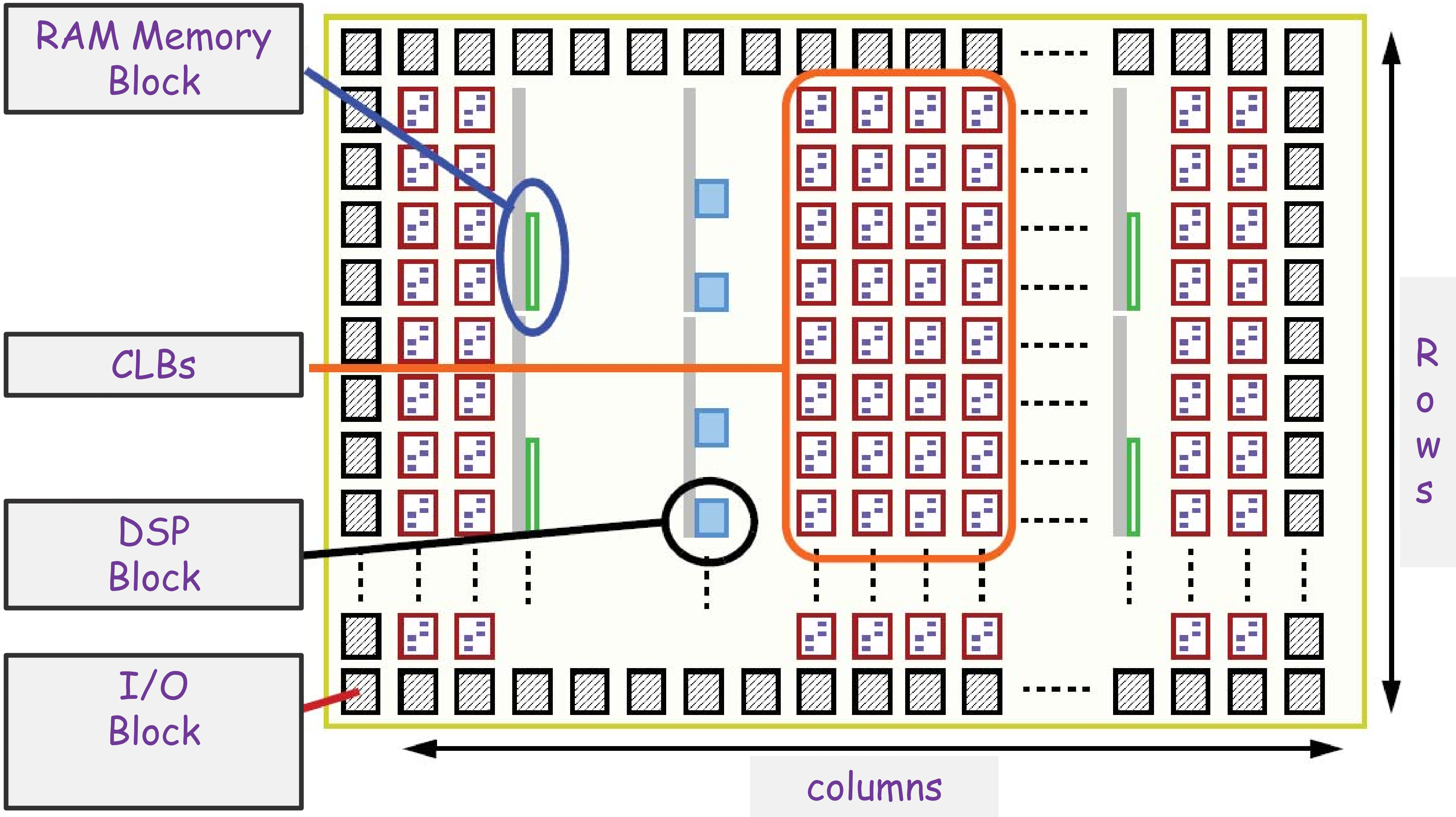
FPGA? – What is it?

- Programmable Logic, Interconnections and Routing
- Programmable in System (ISP)
- Dedicated Blocks:
  - Memory
  - Clock Control
  - DSP blocks
  - Embedded processor(s)
  - Gigabits serial transmission/reception
  - Ethernet controller
  - Memory controllers

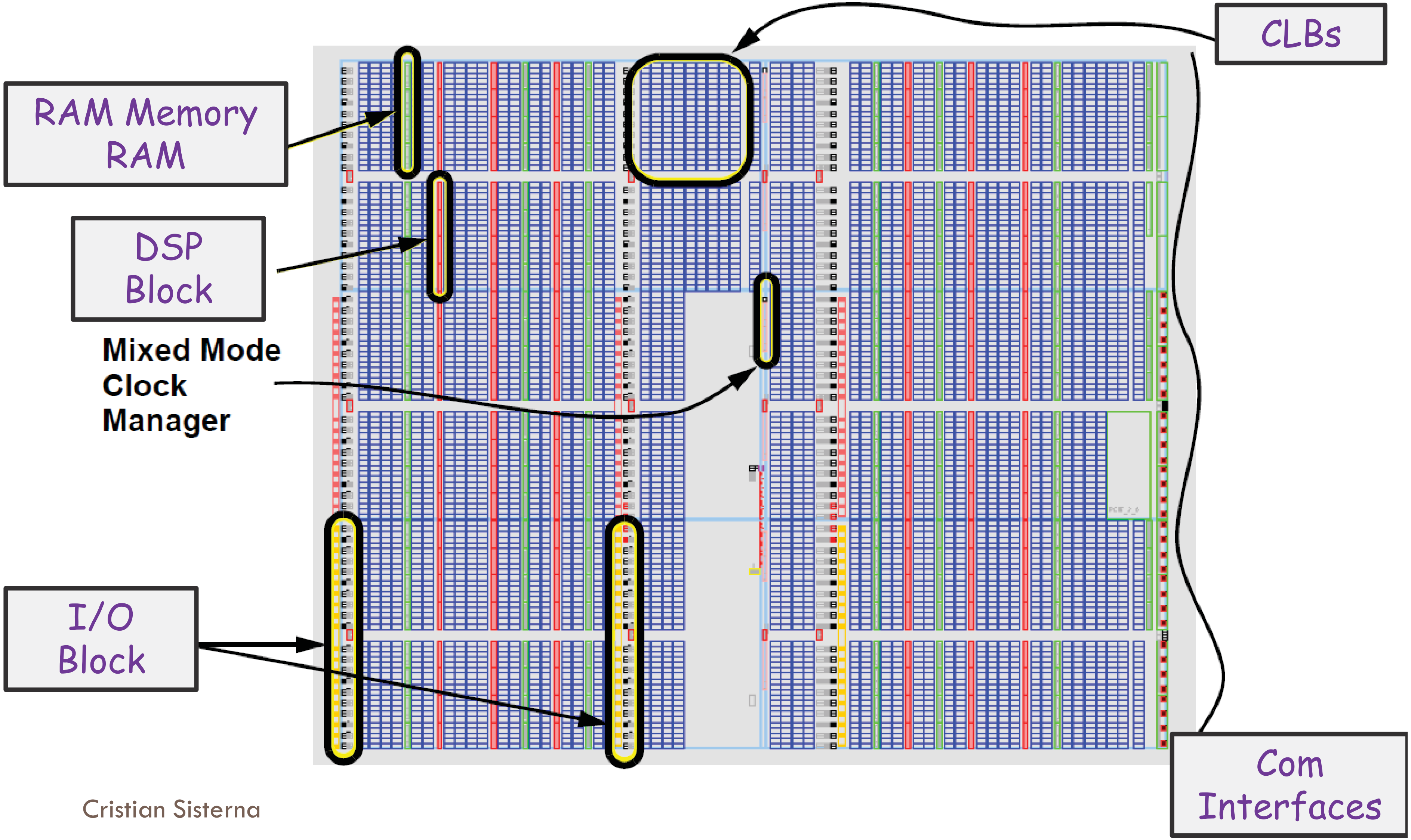
FPGA? – What is it? (cont.)

- Up to1200 I/O
- More than 40 I/O standards. Single ended, Differentials
- More than 40.000 Flips-Flops and Look-Up-Tables (LUTs)
- Soft-Coded Processors, 8051, ARM3
- PLLs and DLLs available (2-12) per device. Up to 550MHz.
- Programmable output impedance
- Dedicated hard coded blocks:
  - Processors
  - PCI E interface
  - Gigabit transceivers
- Dedicated DSP blocks
- Memory blocks

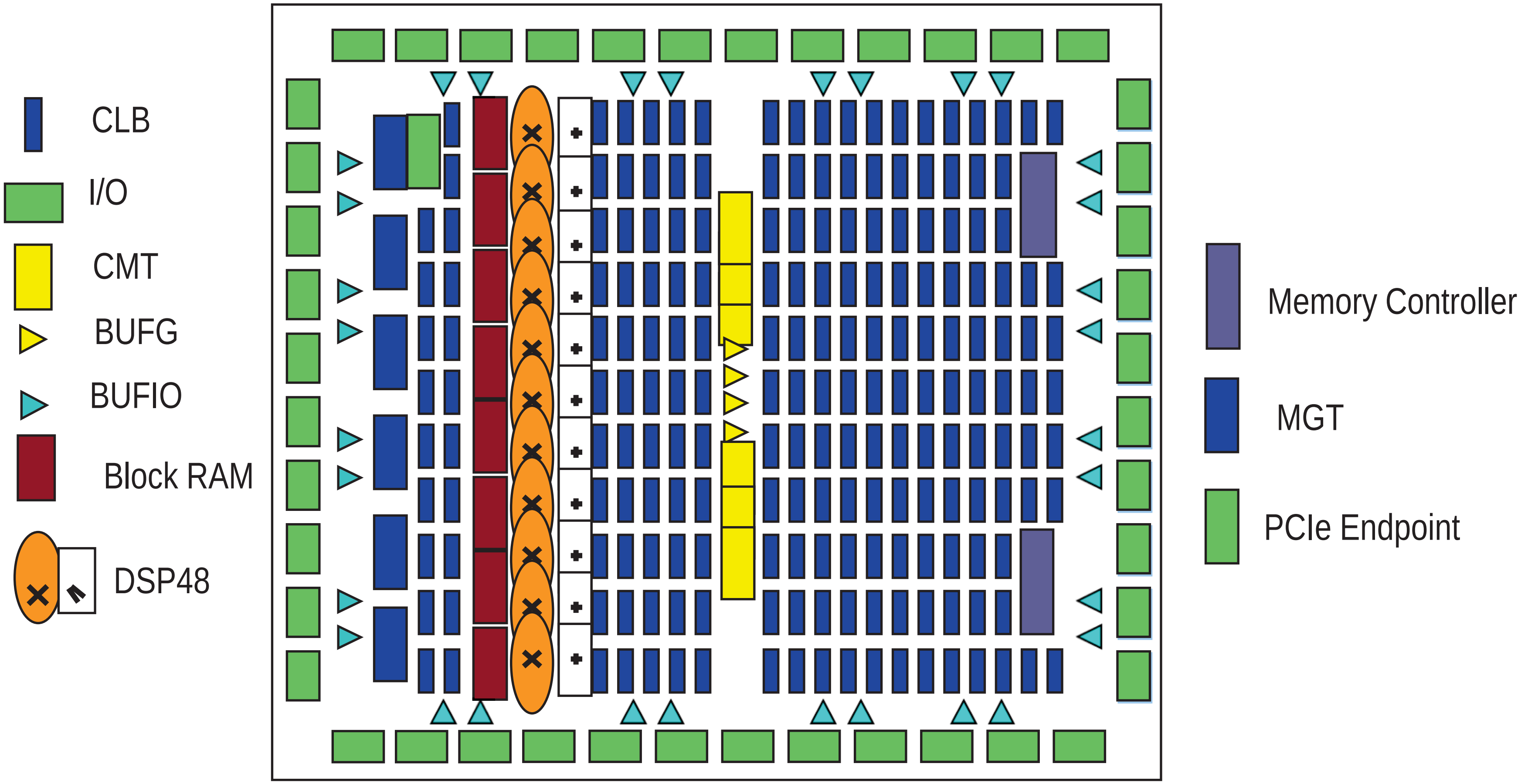
FPGA Architecture



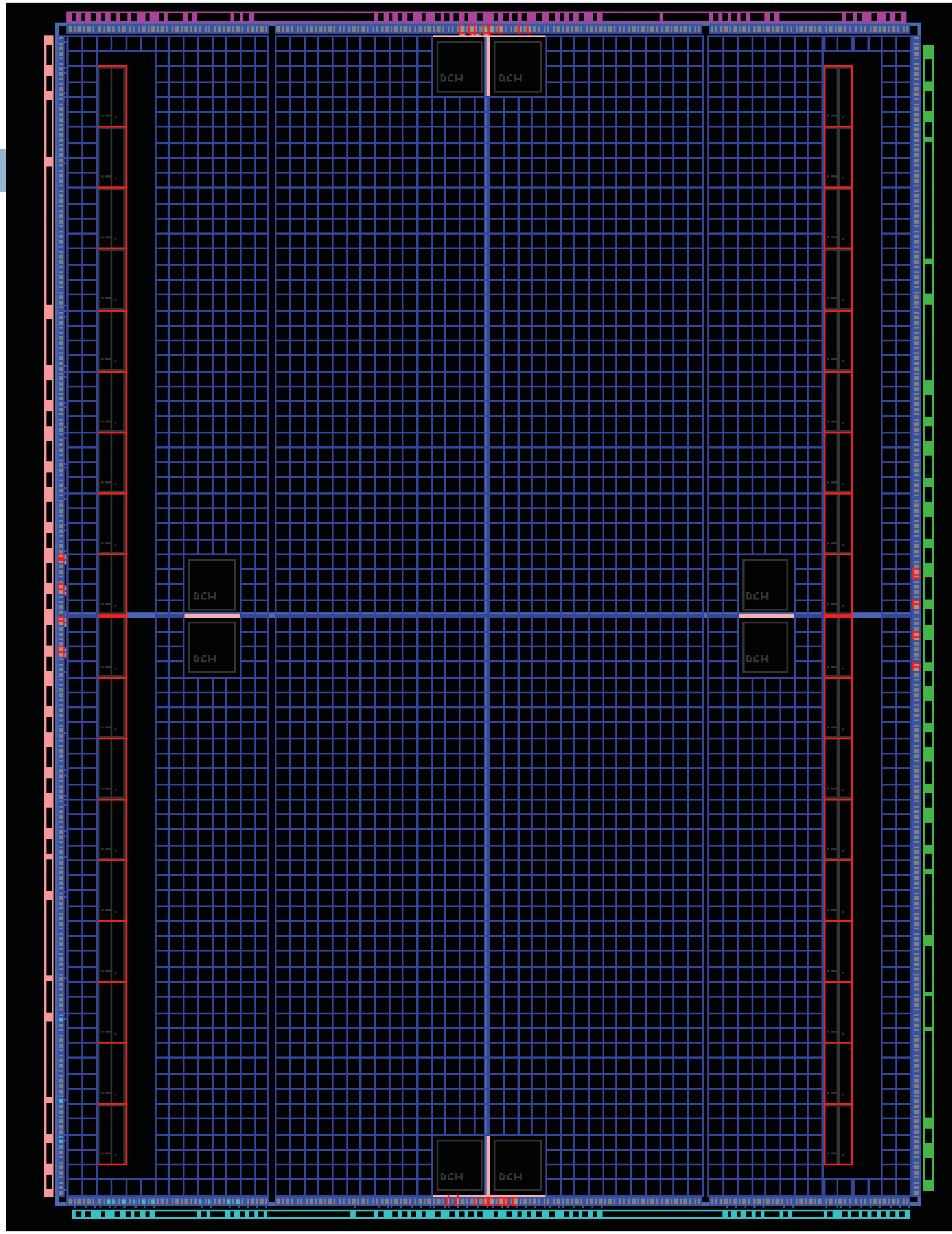
FPGA Architecture (cont.)



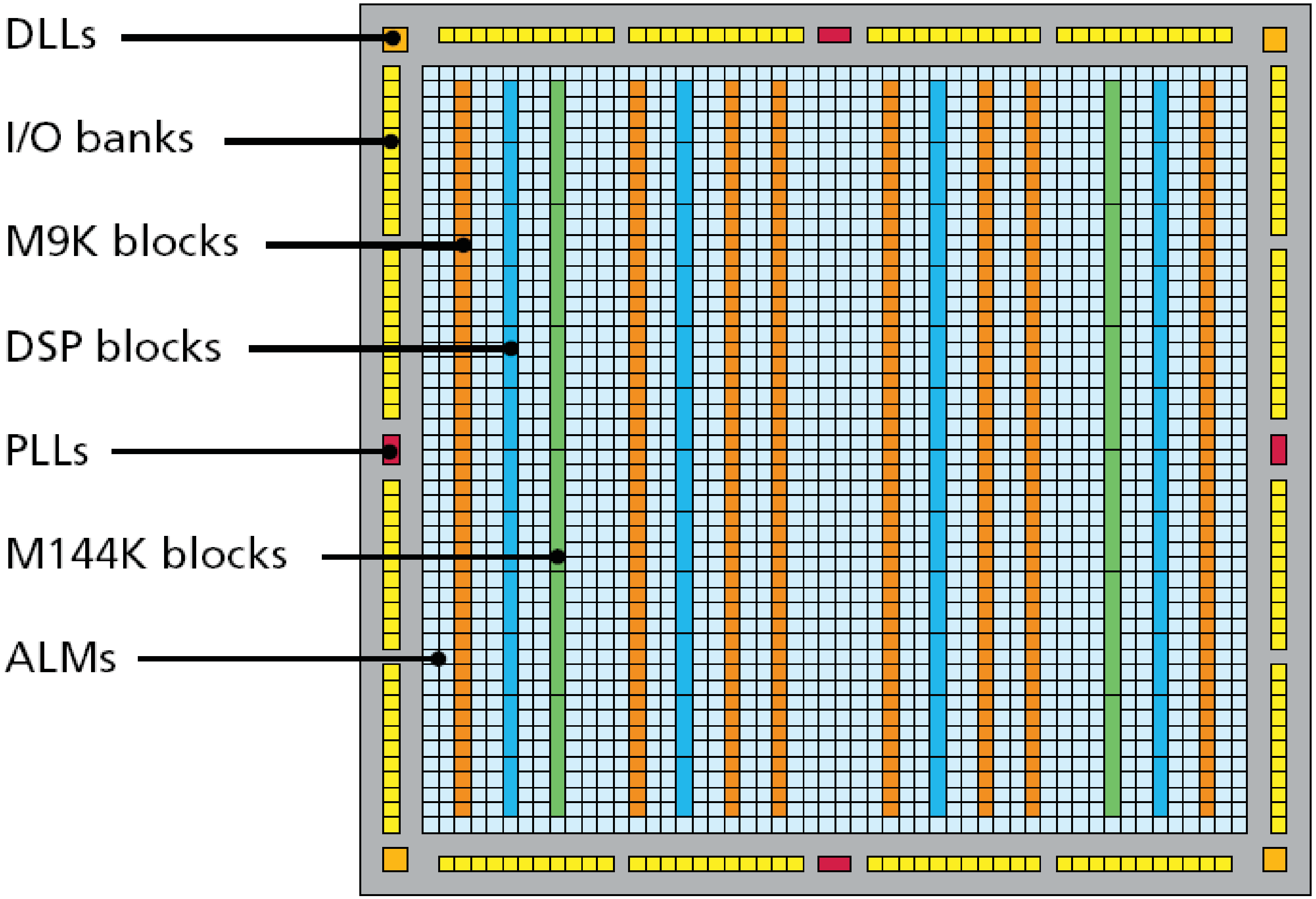
Spartan-6 FPGA Architecture



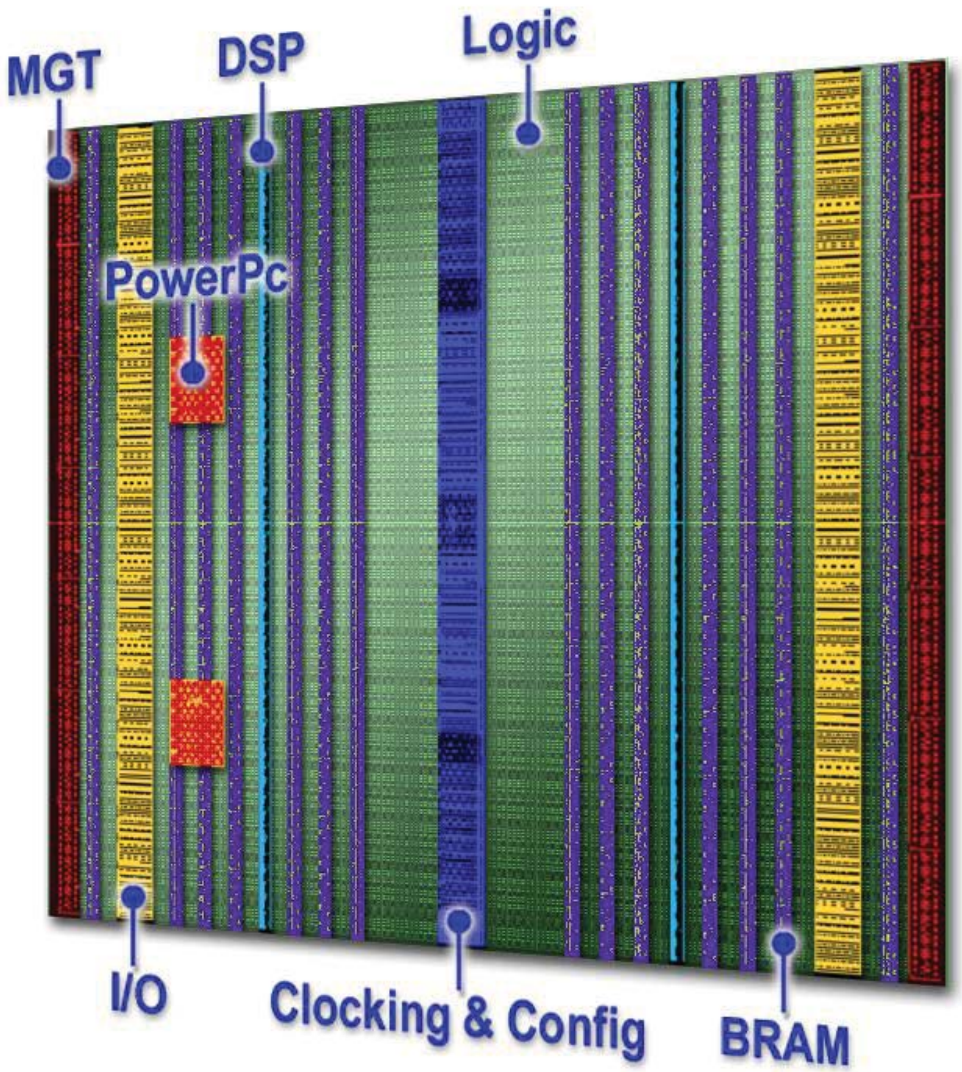
Spartan 3 Internal View



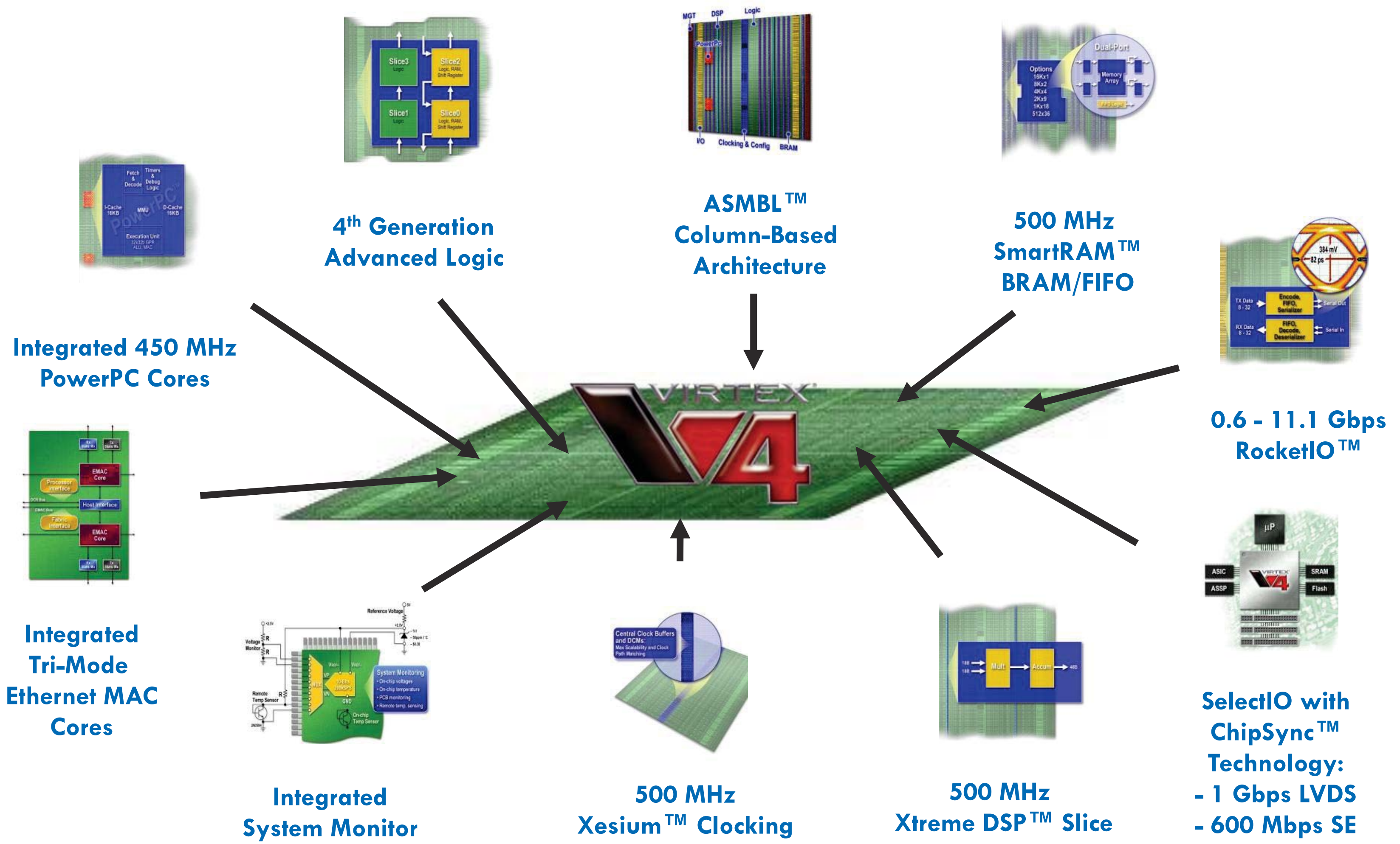
General Altera FPGA Architecture



FPGA Silicon View

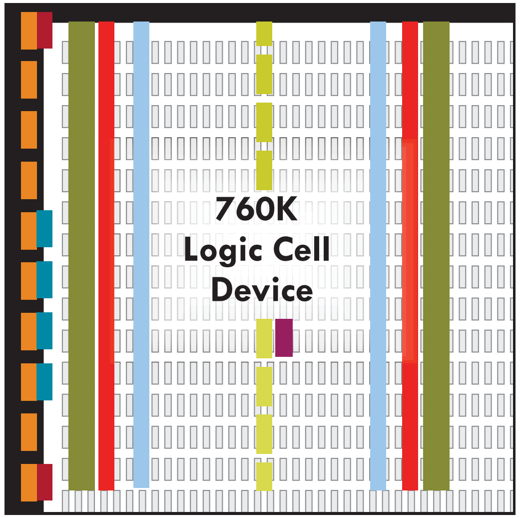


Resources Available in an FPGA

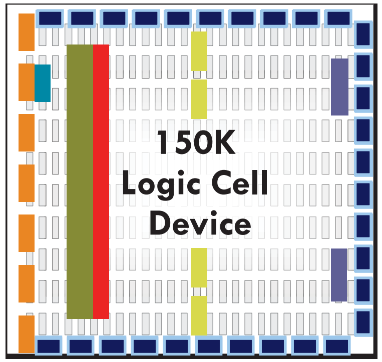


Xilinx FPGA Architecture Alignment

Virtex-6 FPGAs



Spartan-6 FPGAs



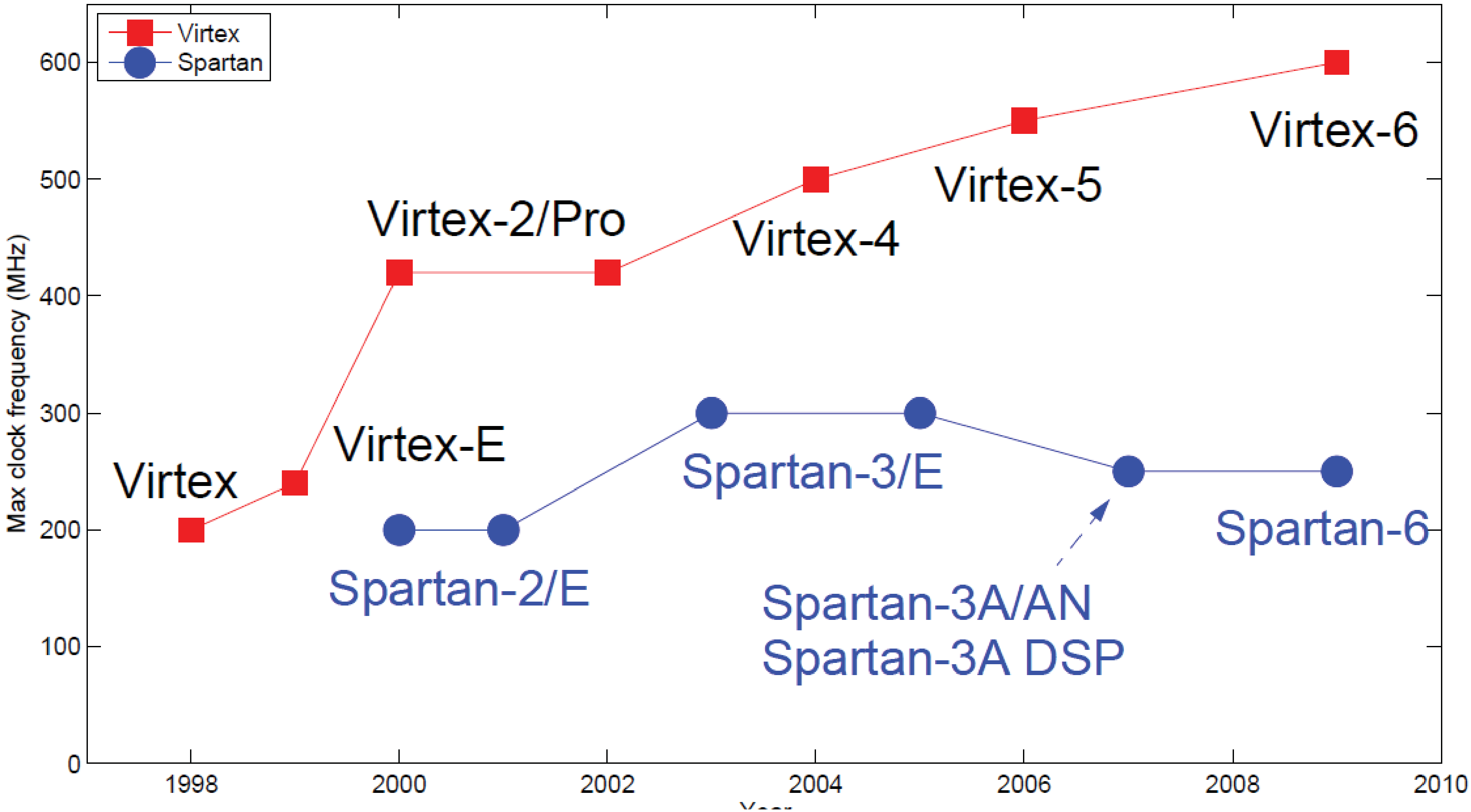
Common Resources

- LUT-6 CLB
- BlockRAM
- DSP Slices
- High-performance Clocking
- Parallel I/O
- HSS Transceivers*
- PCIe® Interface

- FIFO Logic
- Tri-mode EMAC
- System Monitor

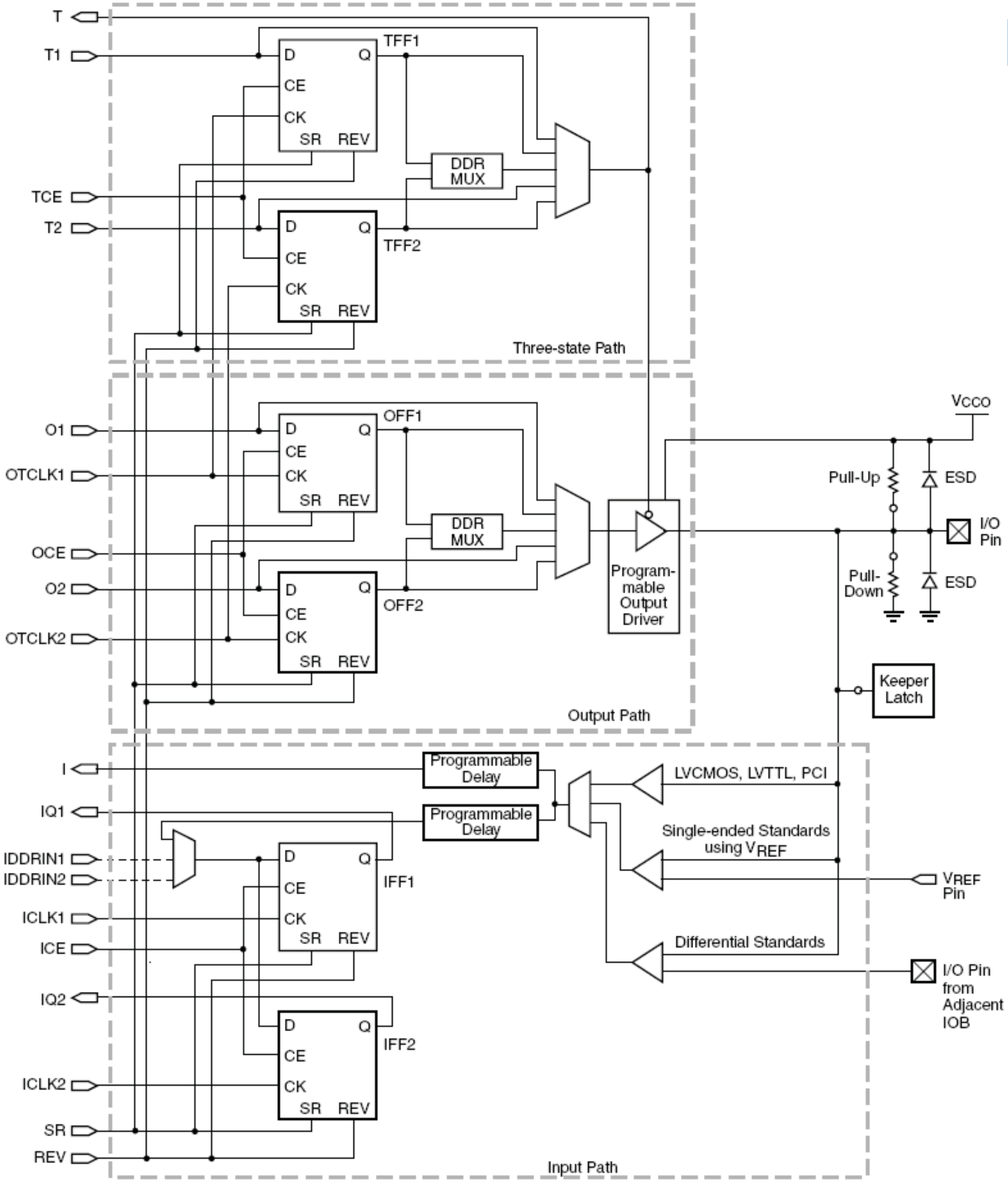
- Hardened Memory Controllers
- 3.3 Volt compatible I/O

Xilinx FPGAs Overview

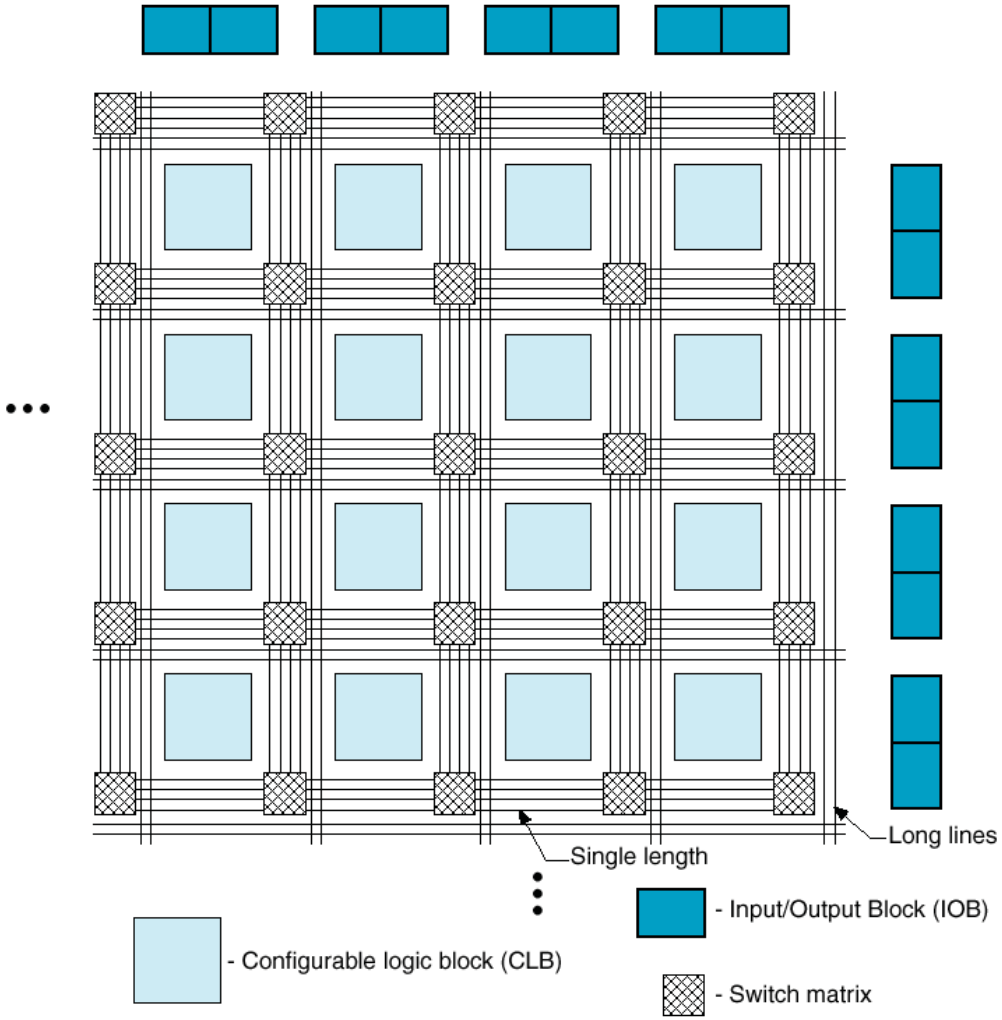


FPGA Configuration and Routing Cell

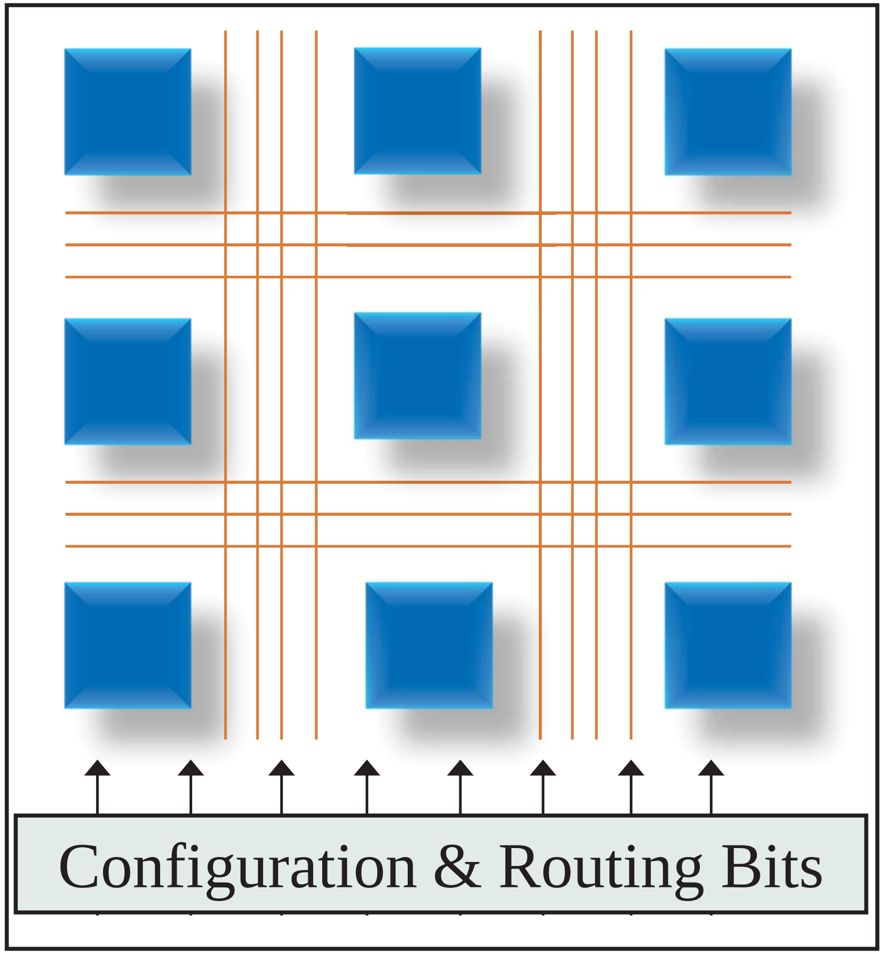
FPGA Logic Configuration Options

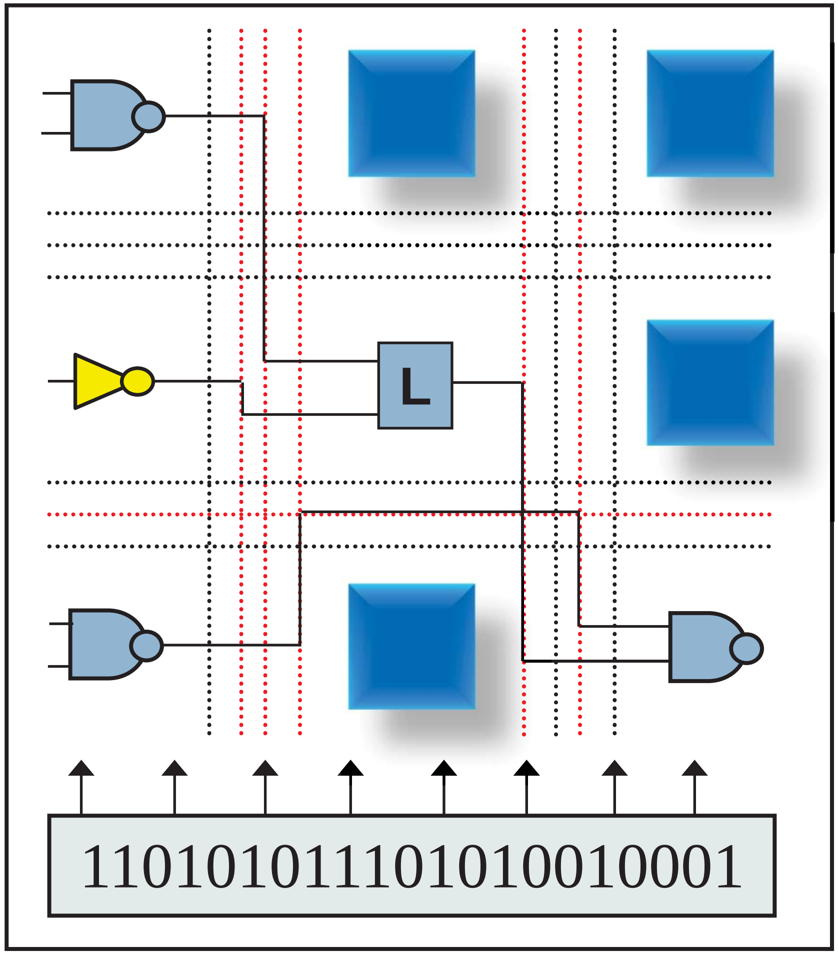


FPGA Routing Options



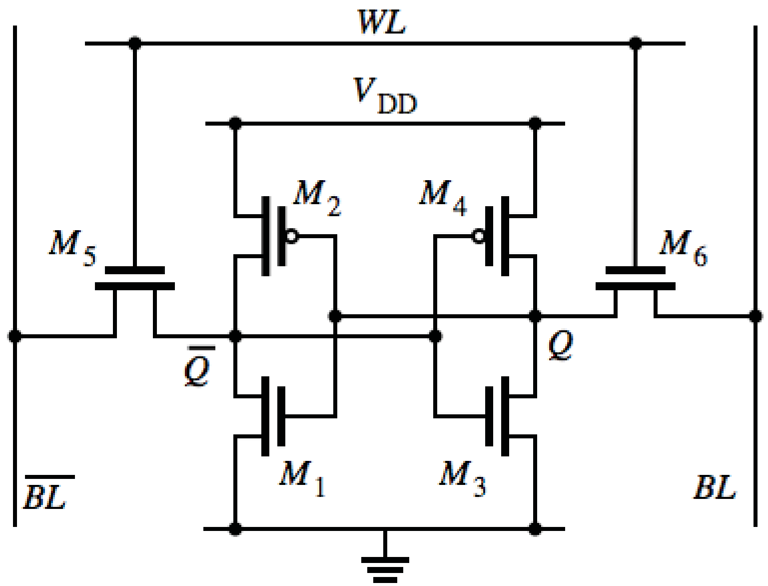
Logic and Routing Configuration

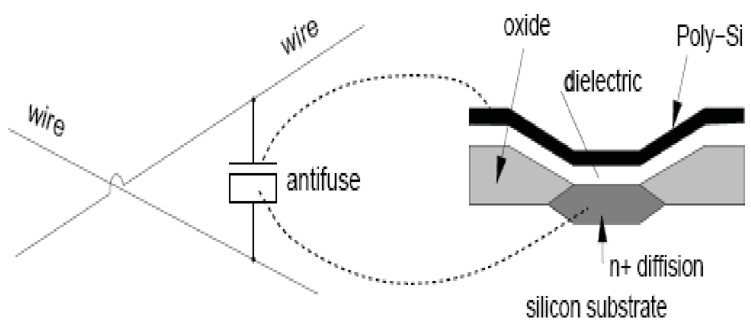


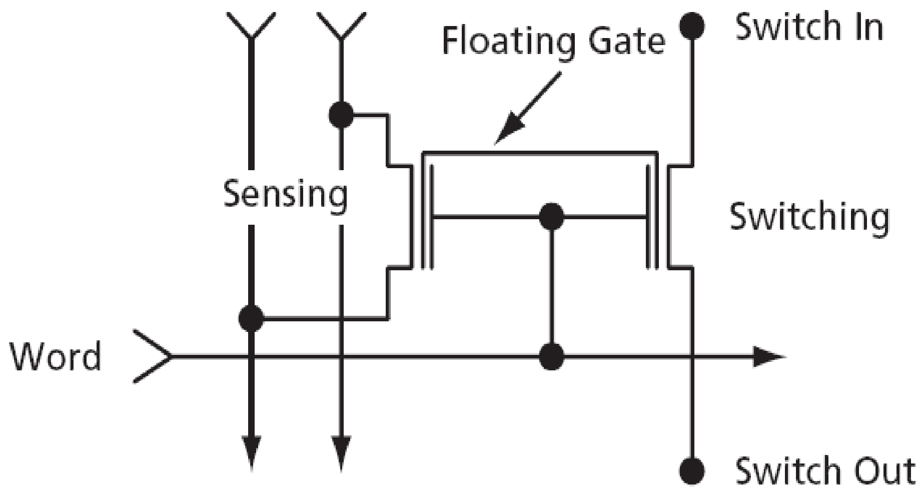


FPGA Configuration Cells

- Tipos de Celdas
  - SRAM
  - Anti-Fuse
  - Flash
  - Flash y SRAM







FPGA Cell Comparison

	SRAM	Anti_fuse	Flash
Technology	Latest	One or Two generation behind	One or Two generation behind
Speed	Slower	Faster	Slower
Volatility	yes	No	No
Power	Poor	Better	Medium
Density	Good	Best	Medium
Radiation Tolerant	Poor	Best	Medium
External Configuration	Yes	No	No
Cell size	1	1/10	1/7
Reprogrammable	Yes	No	Si
Instant-On	No	Yes	Yes
Security	Poor	Very Good	Very Good
Config. Transistors	6 Transistors	Tiny	2 transistors

FPGA Architecture: Big Fight

In general the FPGA arquitecture is similar among the largest vendors. Even though each vendor states the its FPGA is the BEST. . .

Who is the big winner of this fight?????

The final user

FPGA Architecture

The FPGAs from Xilinx are divided in

Spartan 2-3-6

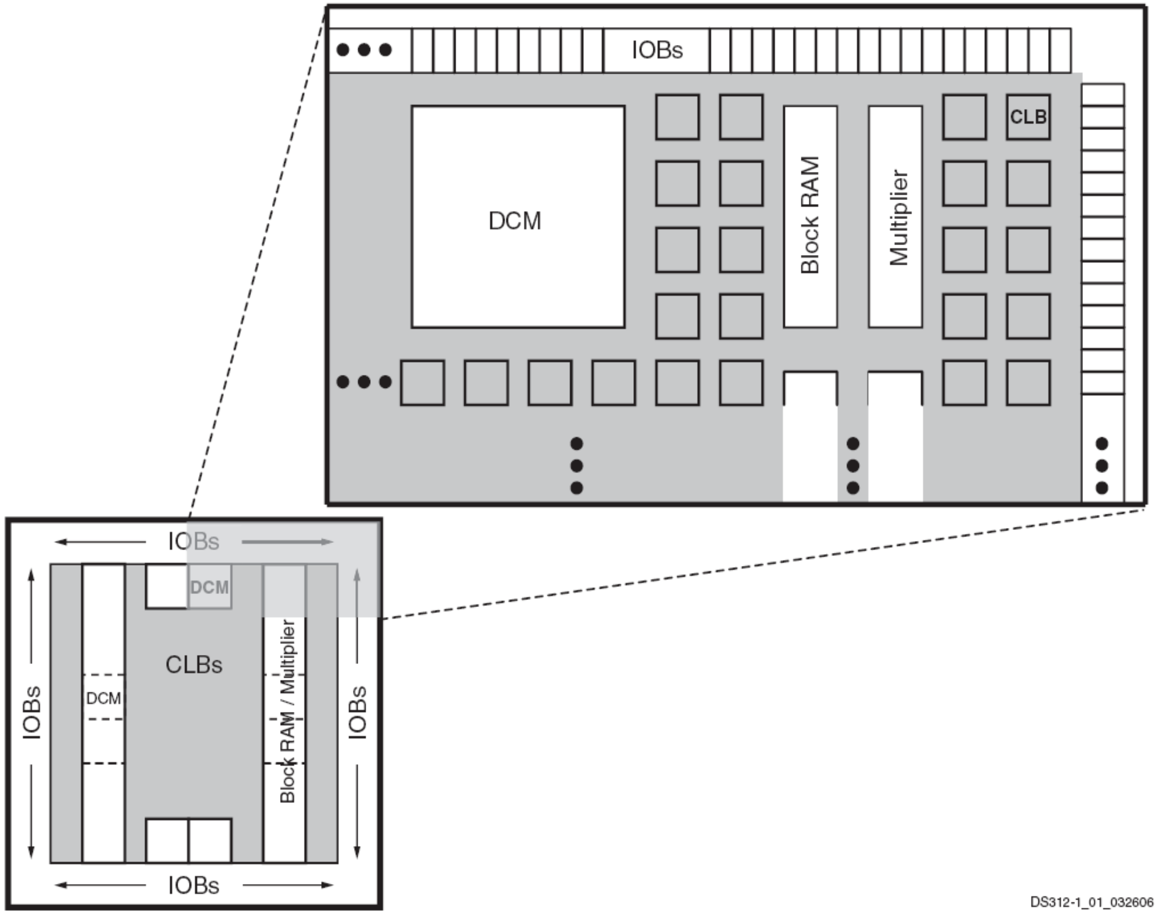
Good performance
Great relation price/performance

Virtex 2-2P-4-5-6

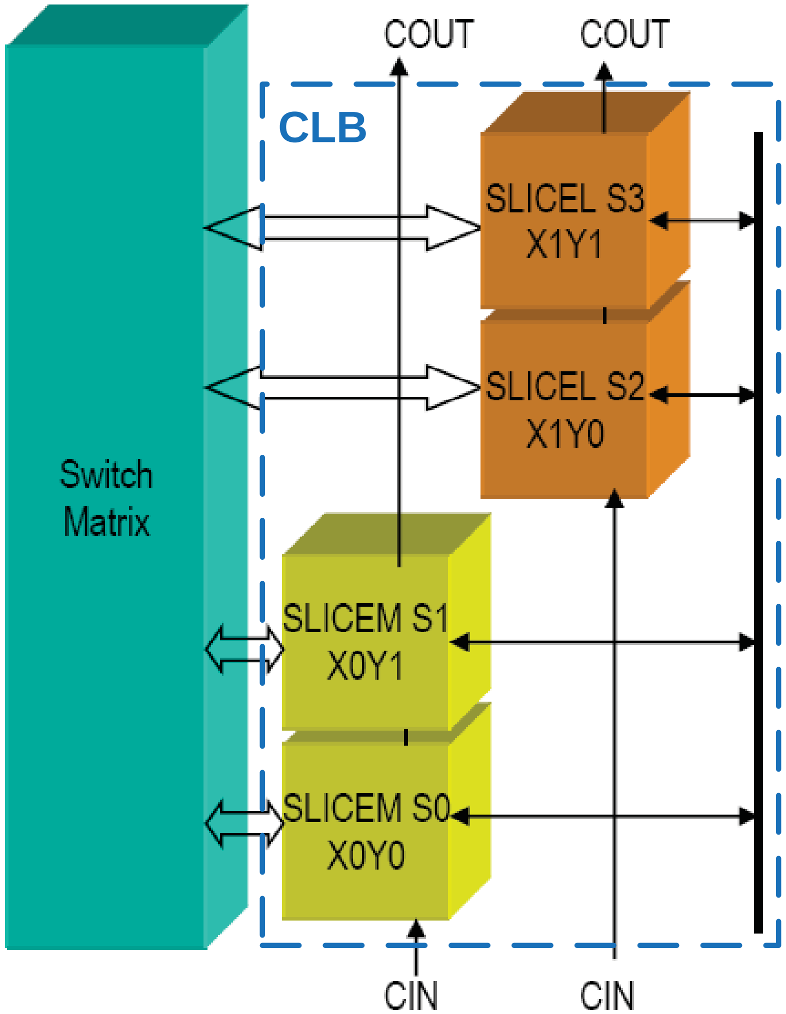
High performance
Expensive

CLB SLICEs

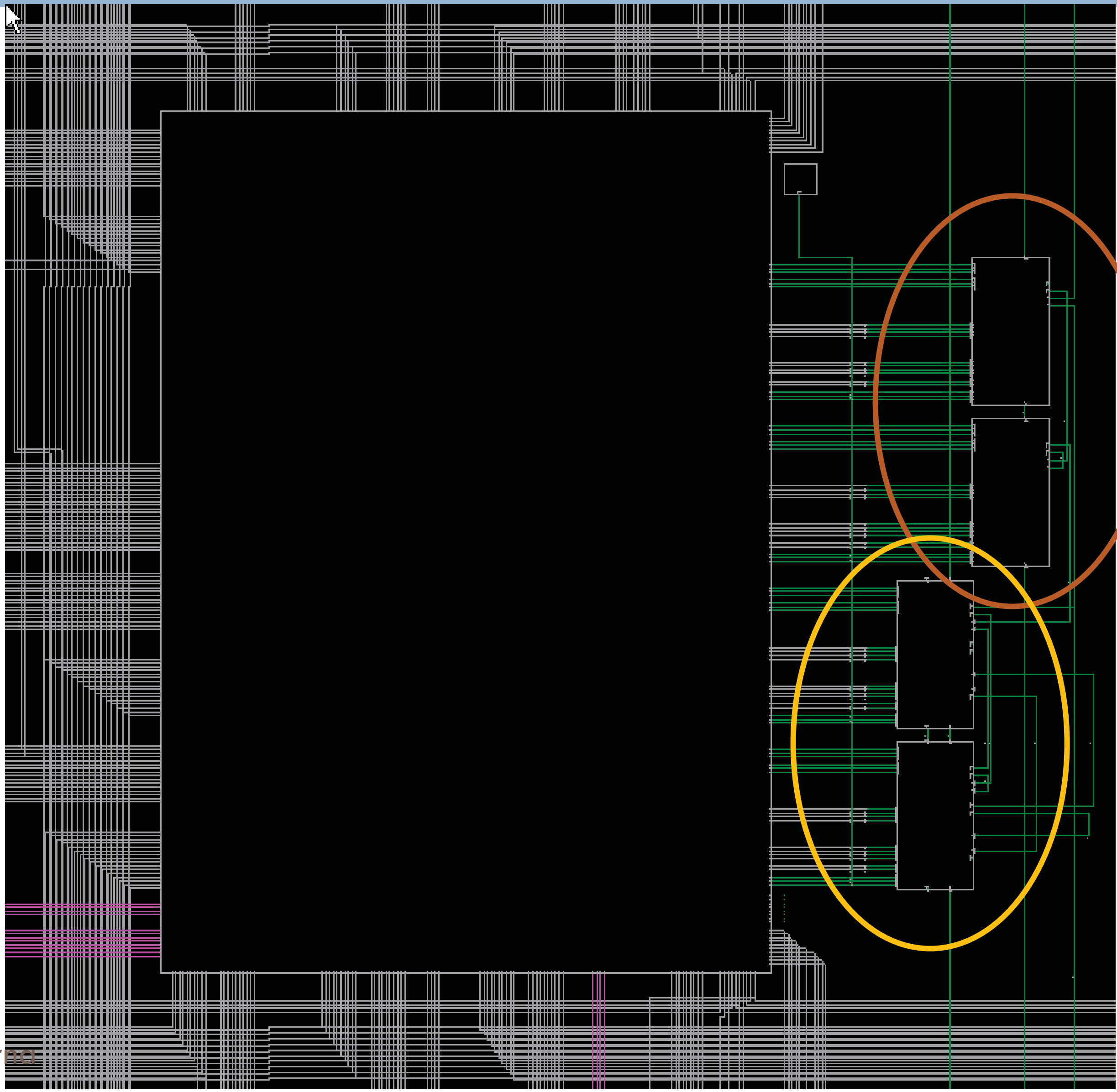
Spartan 3 – FPGA



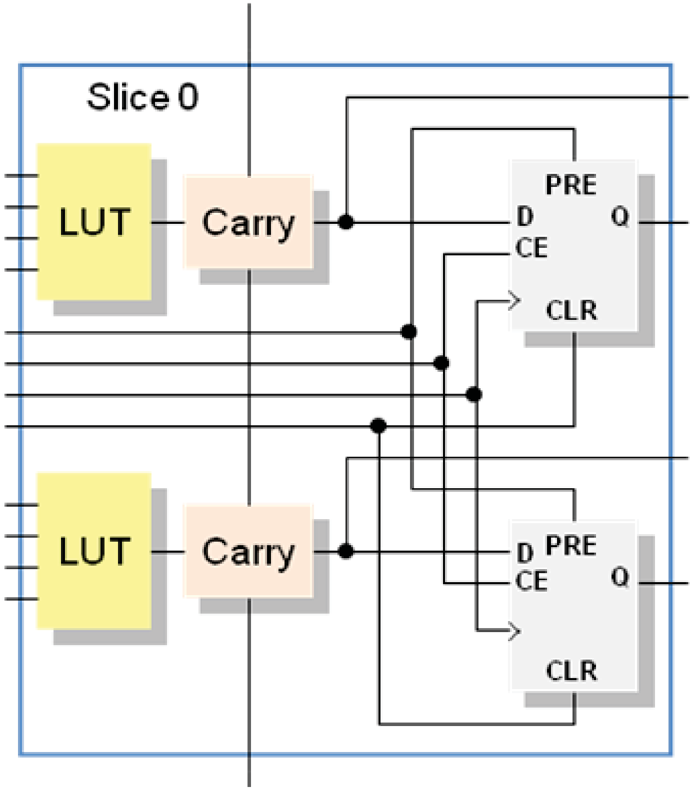
S3 - Configurable Logic Block (CLB)



S3 - CLB – Actual Internal View

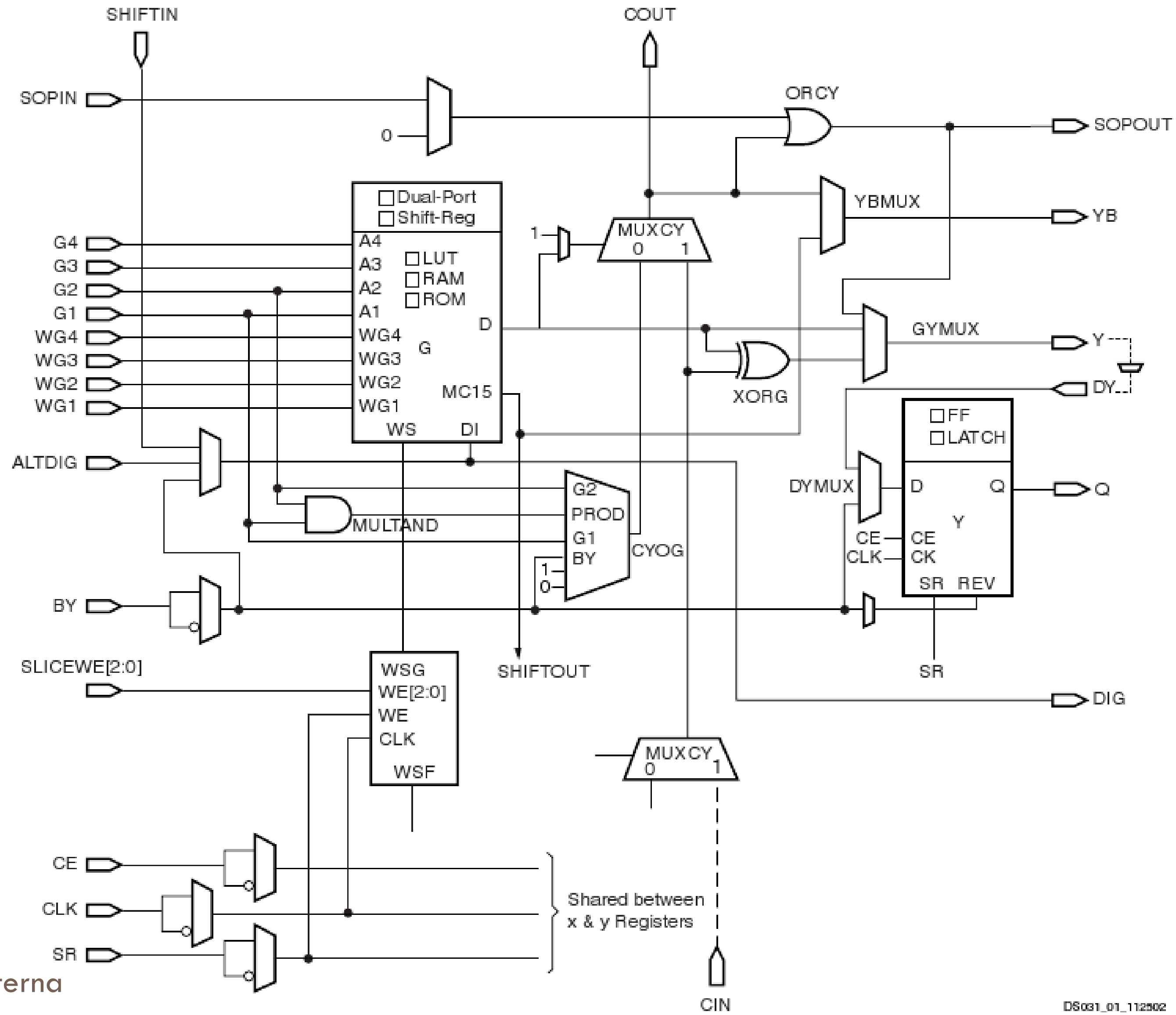


S3 - CLB – Main Logic

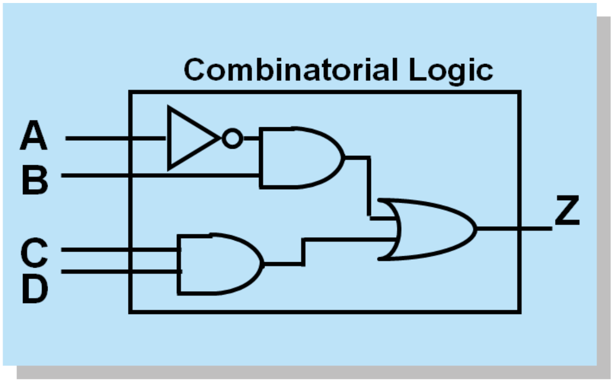


- Two LUTs
- Tow flip-flops
- Four outputs
  - Two combinationals
  - Two registered
- Control Input for FFs
-
- I/O carry chain

S3 – Half Slice Detailed View



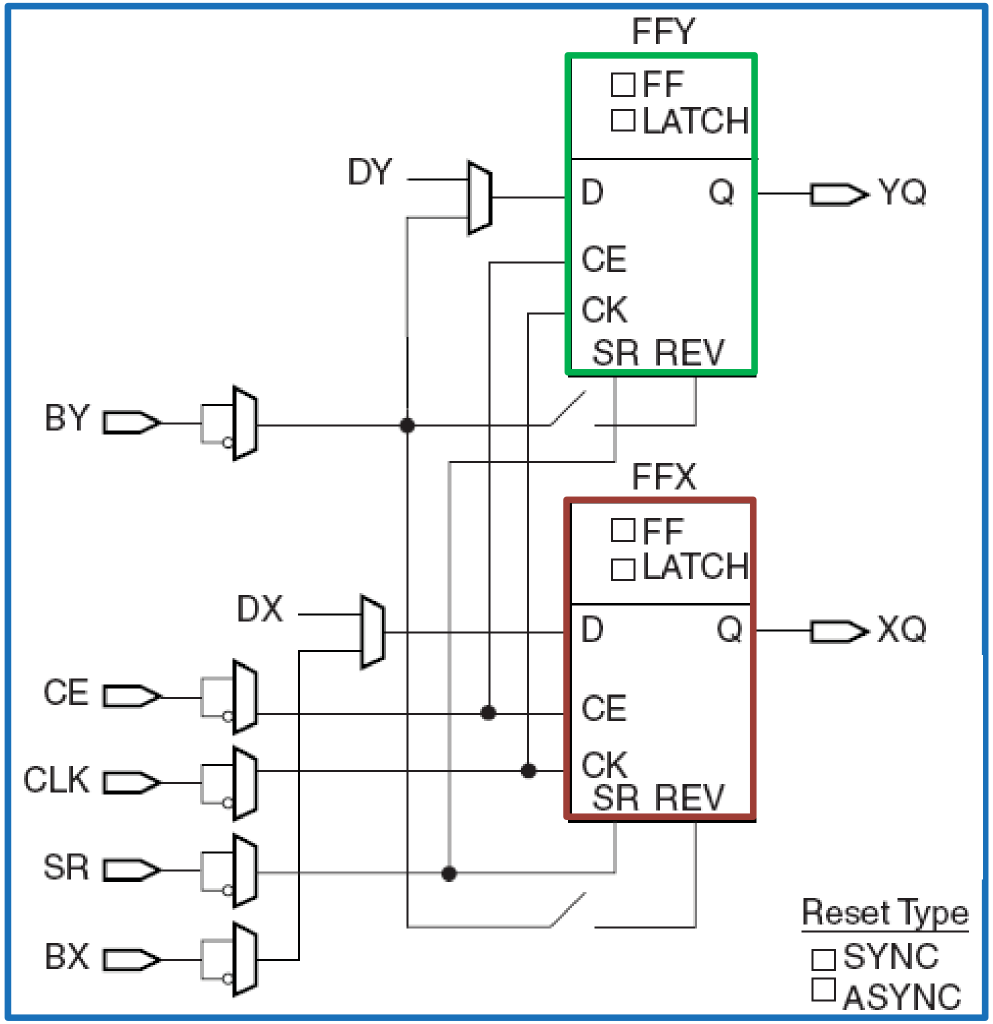
S3 - Look-Up Table



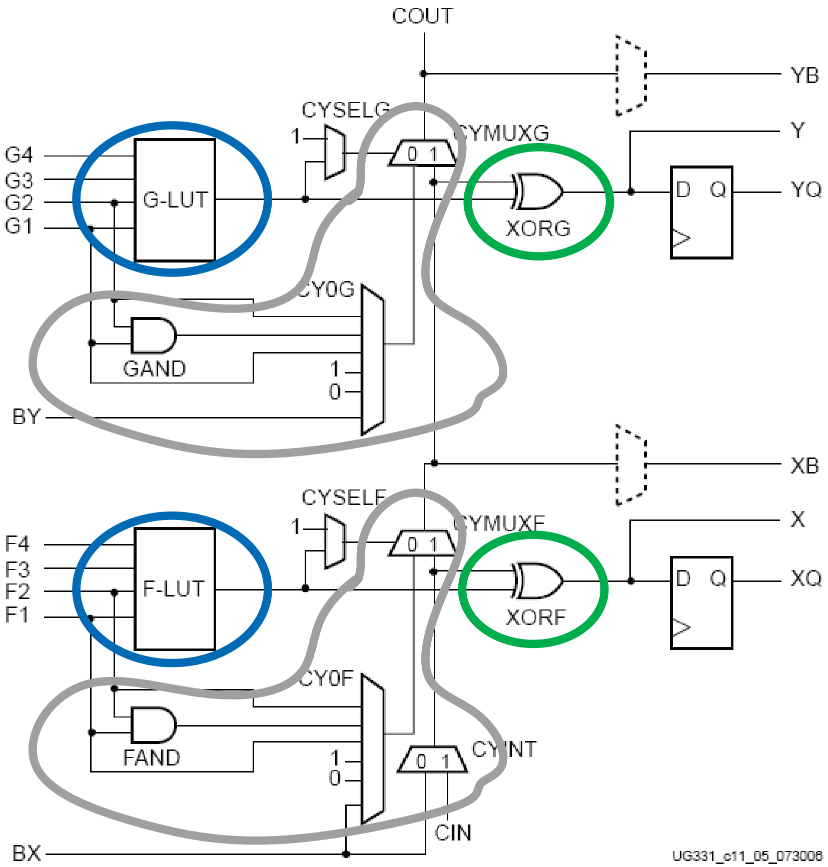
A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

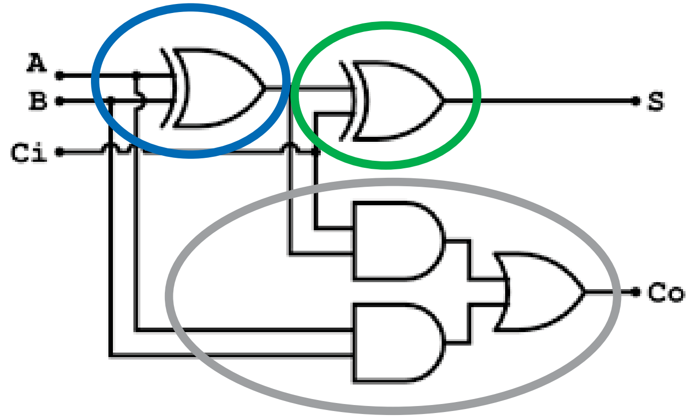
The LUT configuration is not responsibility of the designer

S3 - CLB Register Elements

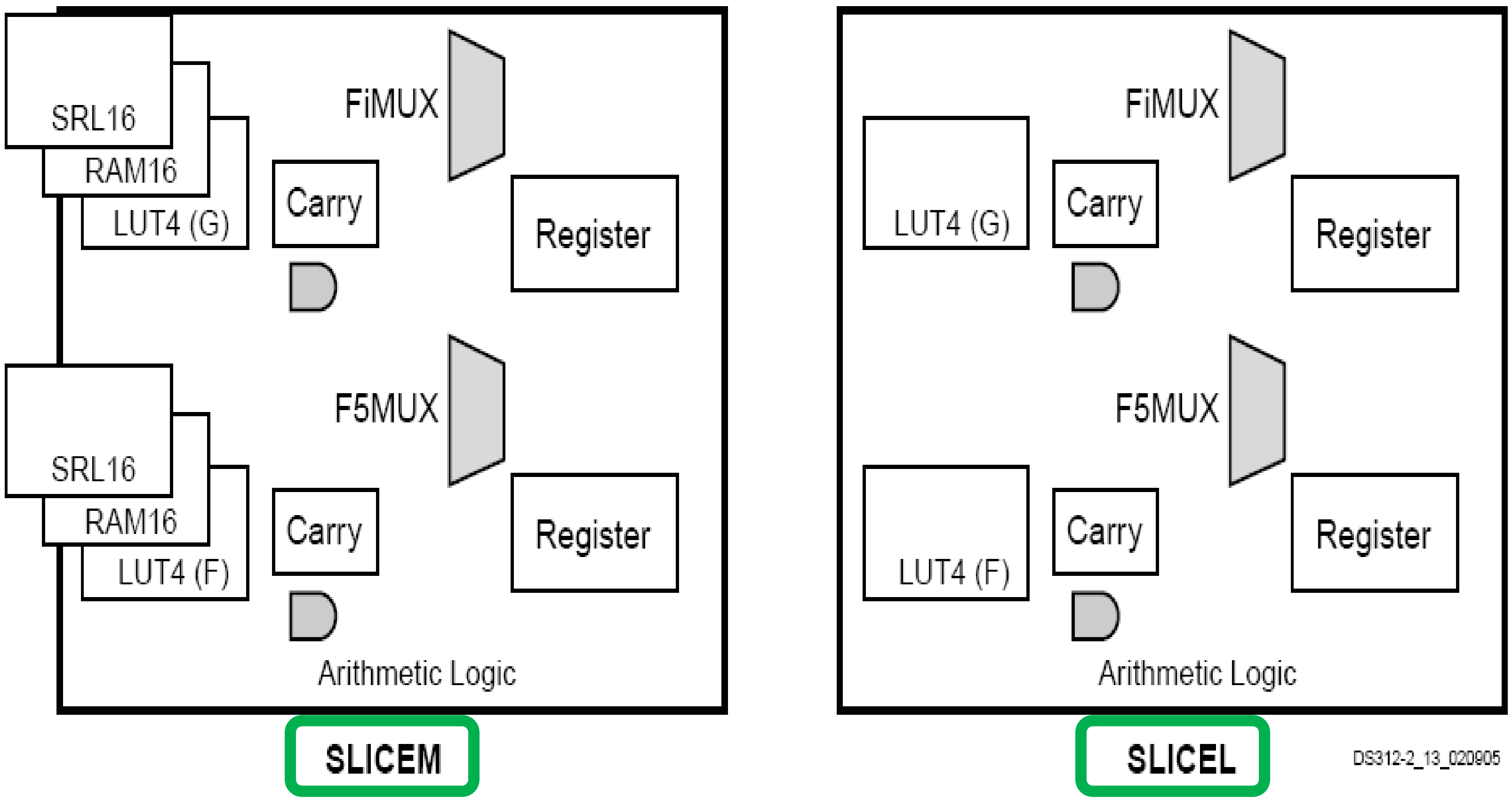


S3 - CLB – Carry Logic

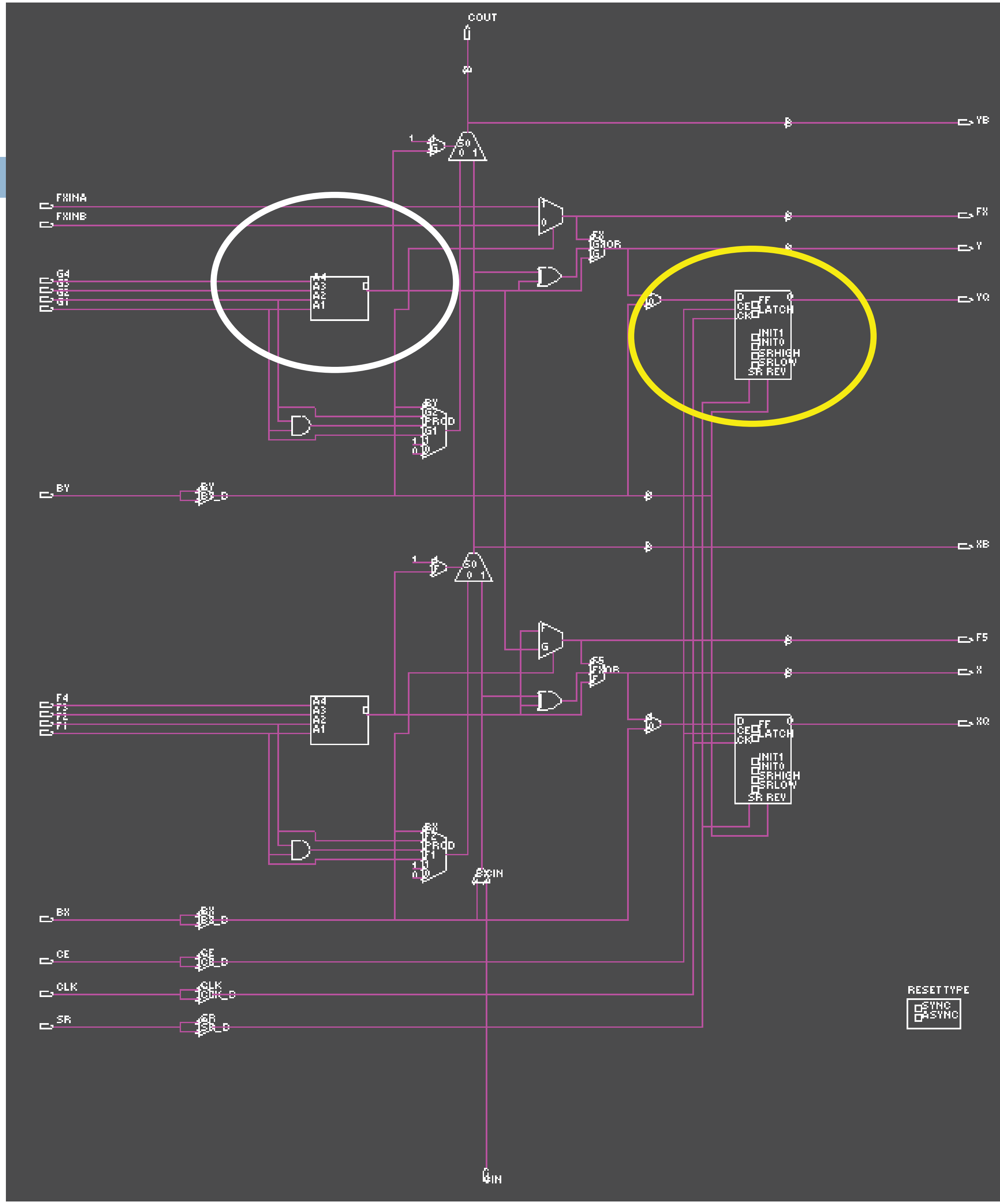




S3 - Different Type of SLICEs

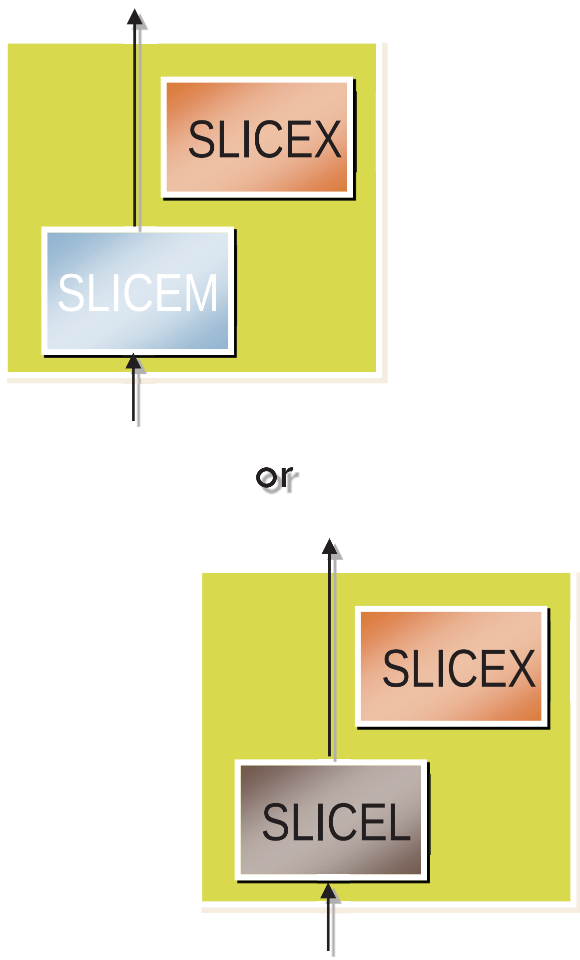


CLB Internal View



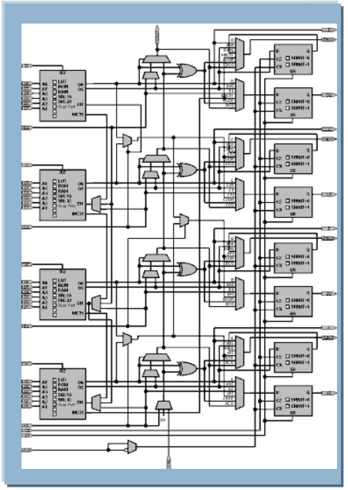
S6 - SLICEs

- **SLICEM:** Full slice
  - LUT can be used for logic and memory/SRL
  - Has wide multiplexers and carry chain
- **SLICEL:** Logic and arithmetic only
  - LUT can only be used for logic (not memory)
  - Has wide multiplexers and carry chain
- **SLICEX:** Logic only
  - LUT can only be used for logic (not memory)
  - No wide multiplexers or carry chain



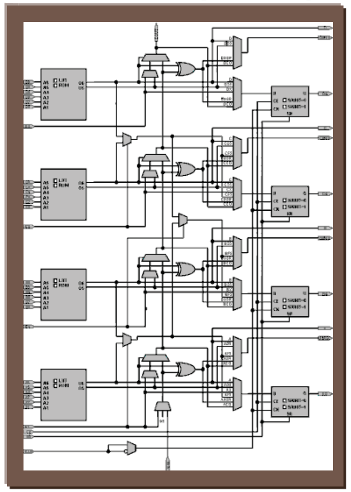
S6 – SLICEs

SliceM (25%)



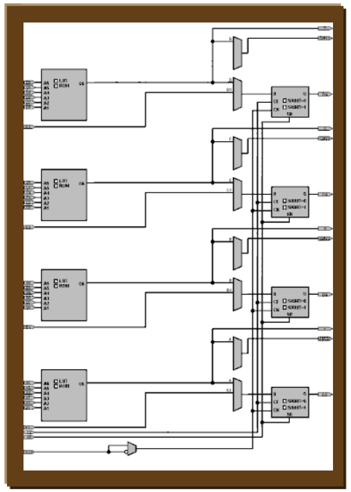
- LUT6
- 8 Registers
- Carry Logic
- Wide Function Muxes
- Distributed RAM / SRL logic

SliceL (25%)



- LUT6
- 8 Registers
- Carry Logic
- Wide Function Muxes

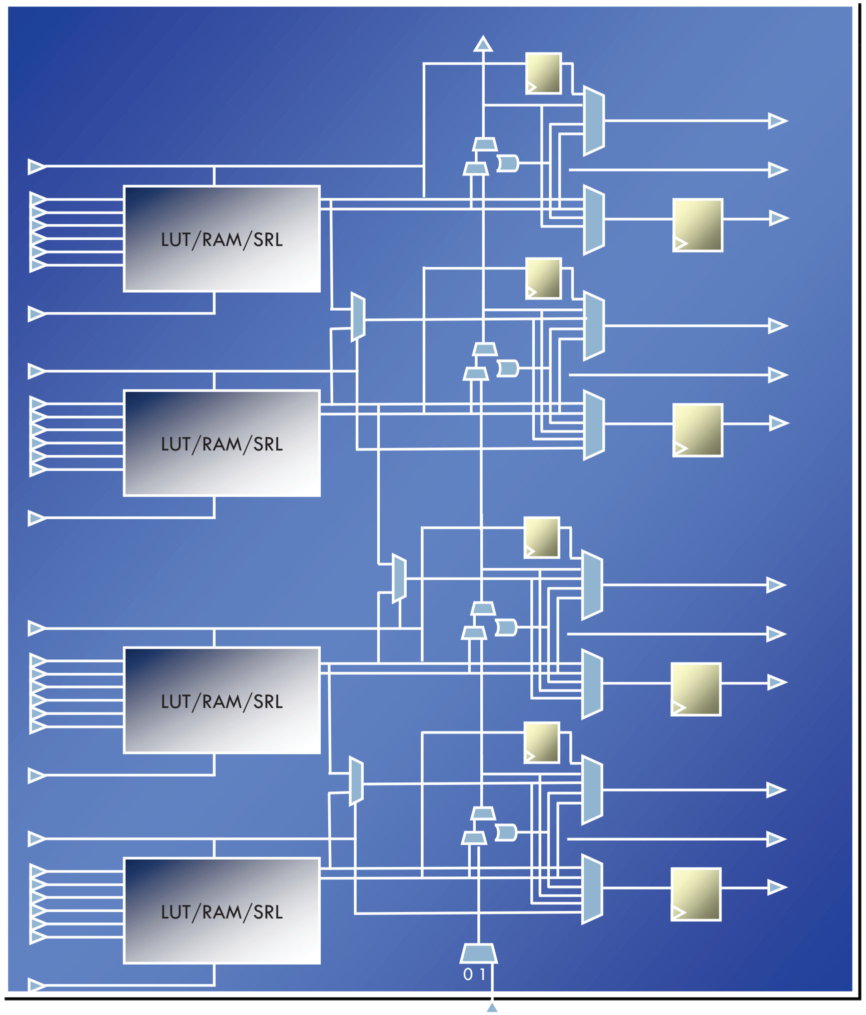
SliceX (50%)



- LUT6
- Optimized for Logic
- 8 Registers

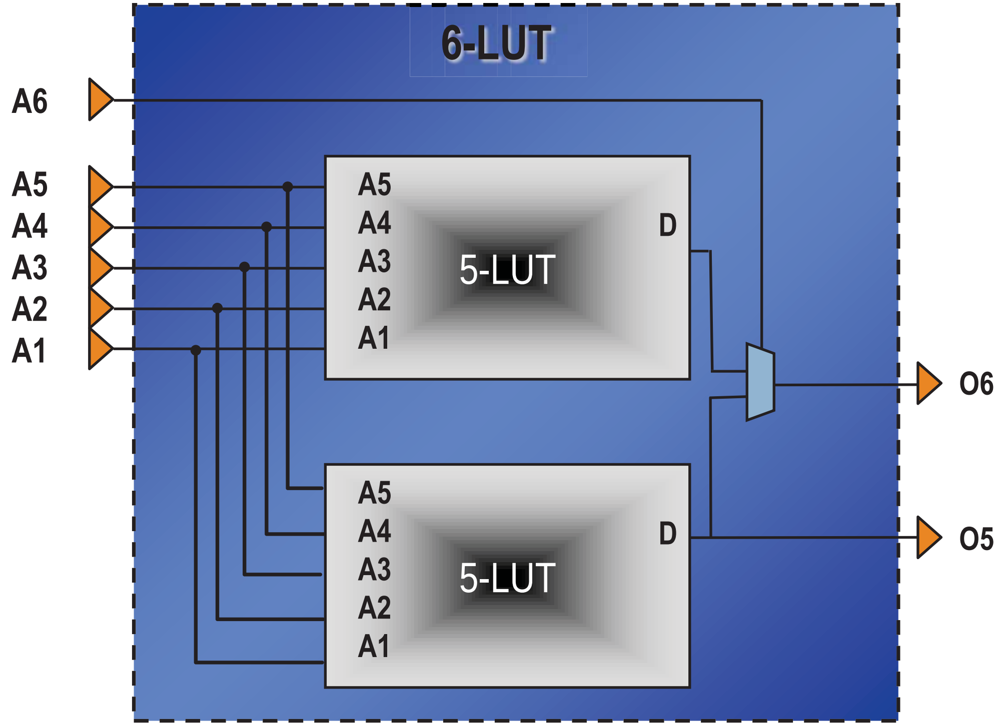
S6 - SLICE

- Four LUTs
- Eight storage elements
  - Four flip-flop/latches
  - Four flip-flops
- F7MUX and F8MUX
  - Connects LUT outputs to create wide functions
  - Output can drive the flip-flop/latches
- Carry chain (Slice0 only)
  - Connected to the LUTs and the four flip-flop/latches

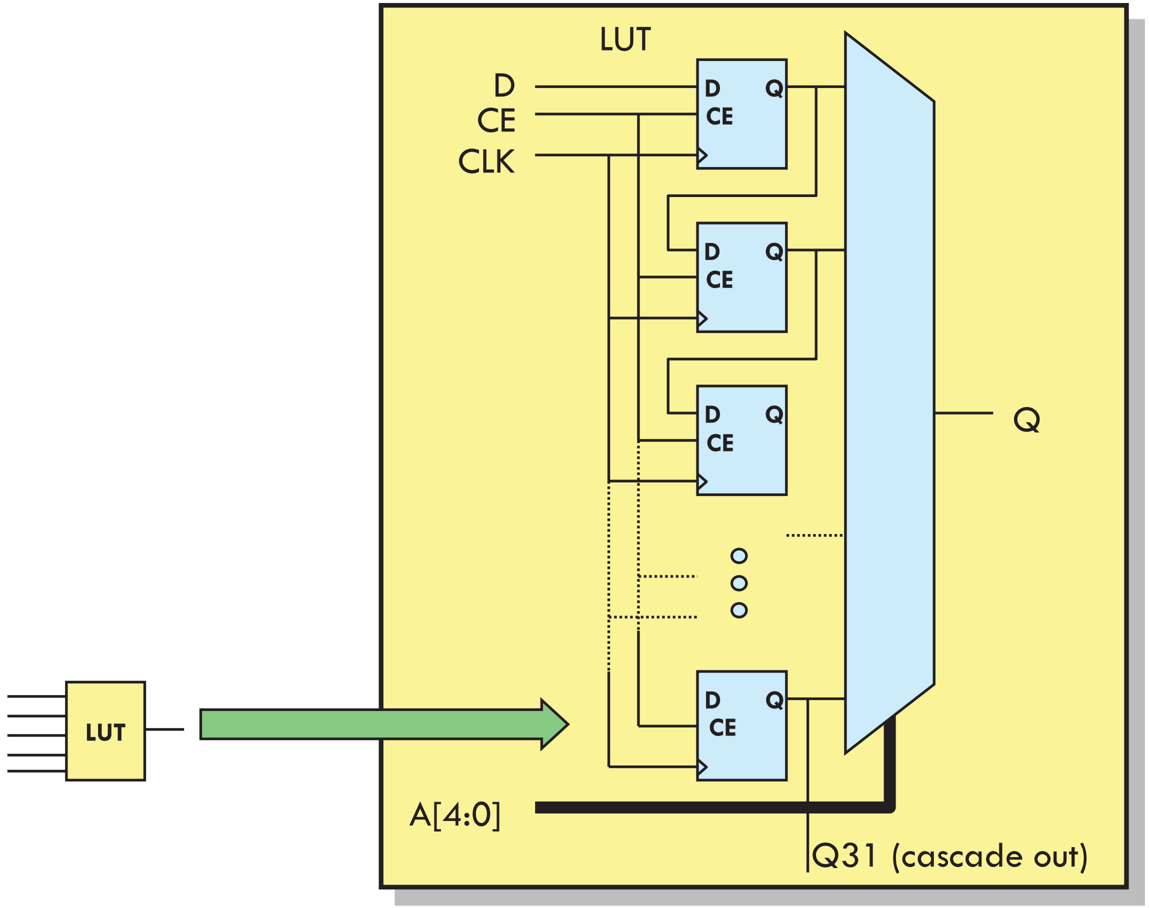


S6 - 6-Input LUT with Dual Output

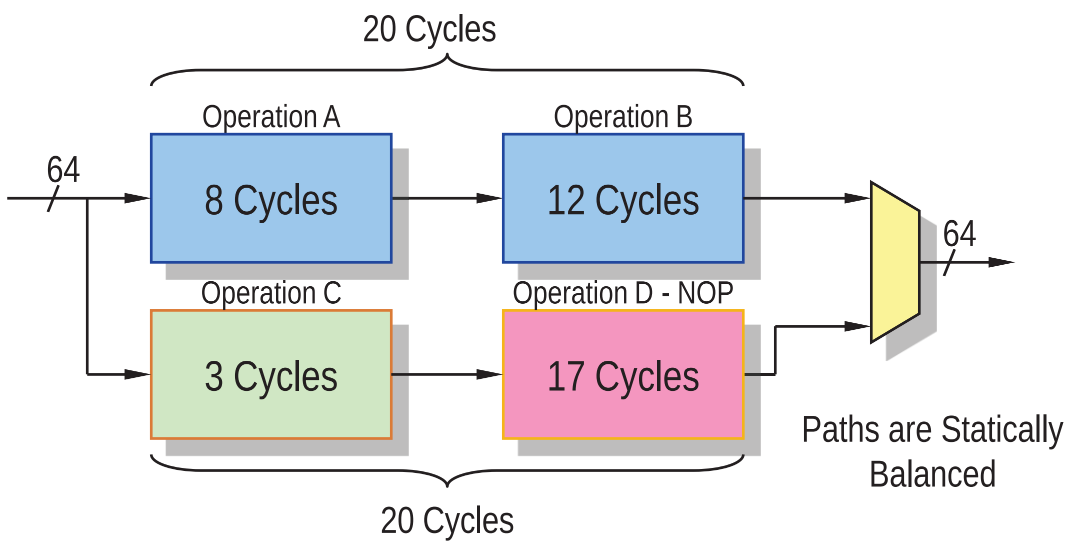
- 6-input LUT can be two 5-input LUTs with common inputs
  - Minimal speed impact to a 6-input LUT
  - One or two outputs
  - Any function of six variables or two independent functions of five variables



Configuring LUTs as a Shift Register (SRL)

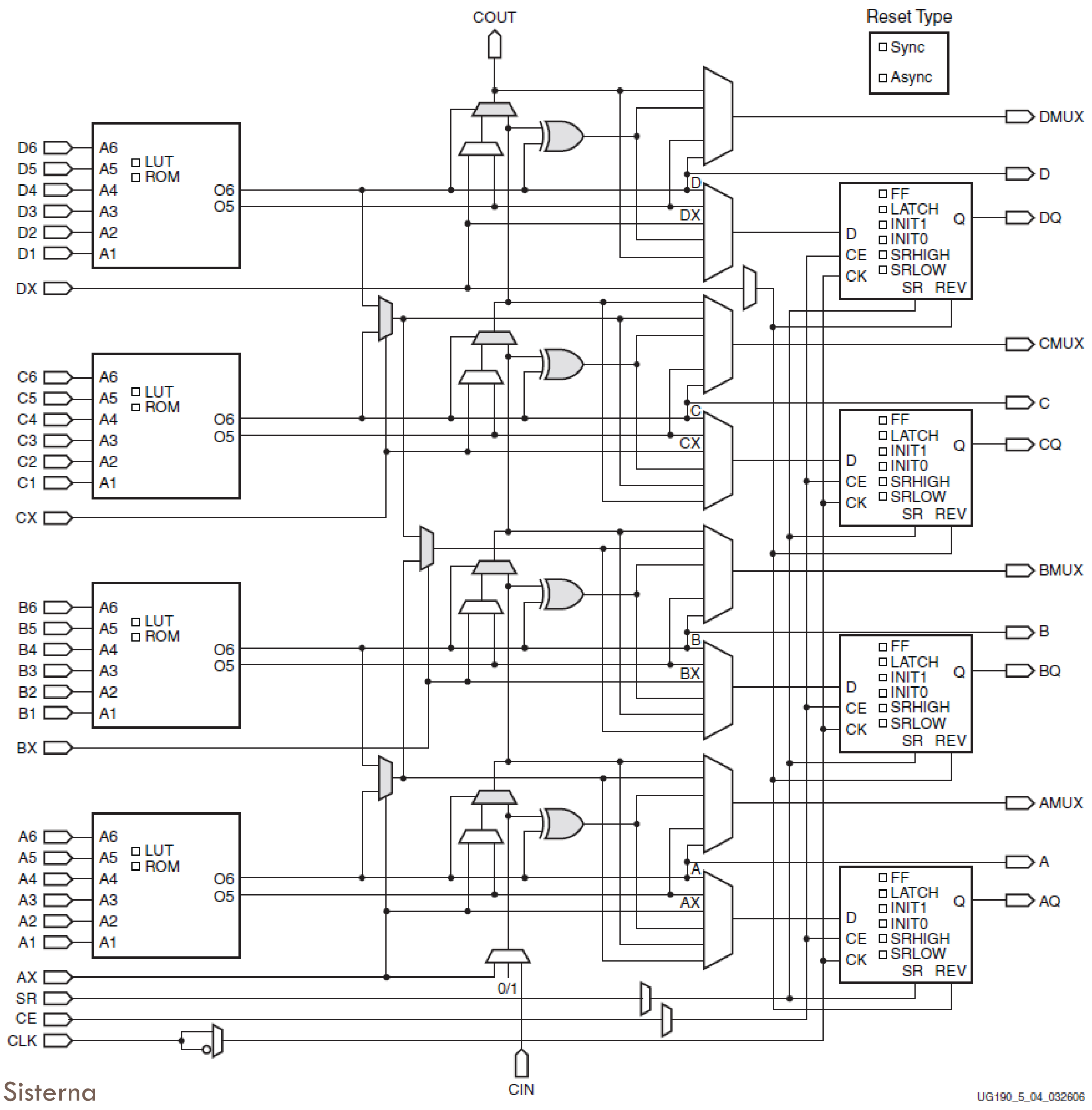


Shift Register LUT Example



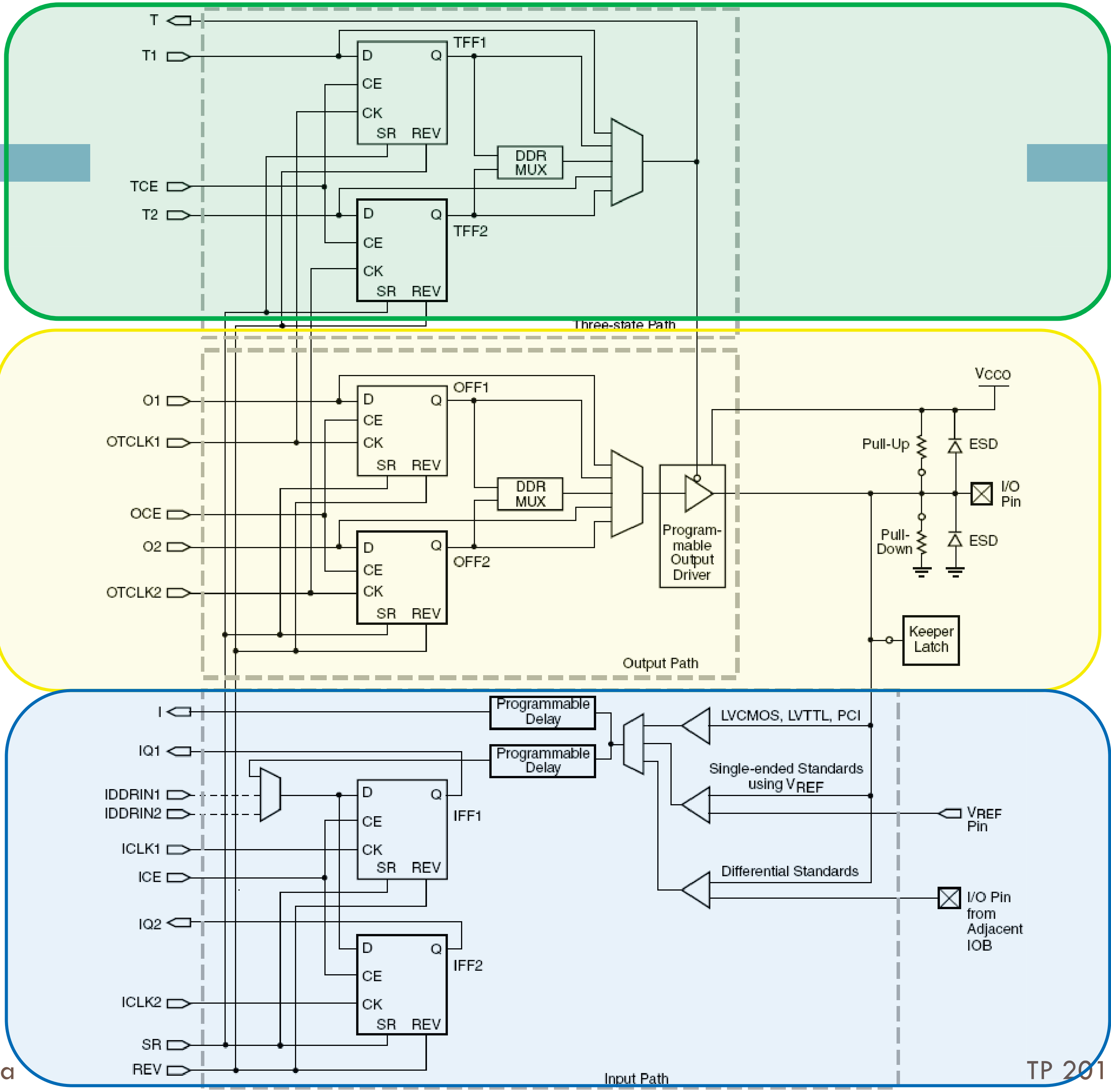
- Operation D - NOP must add 17 pipeline stages of 64 bits each
  - 1,088 flip-flops (hence 136 slices) or
  - 64 SRLs (hence 16 slices)

V5 Slice L

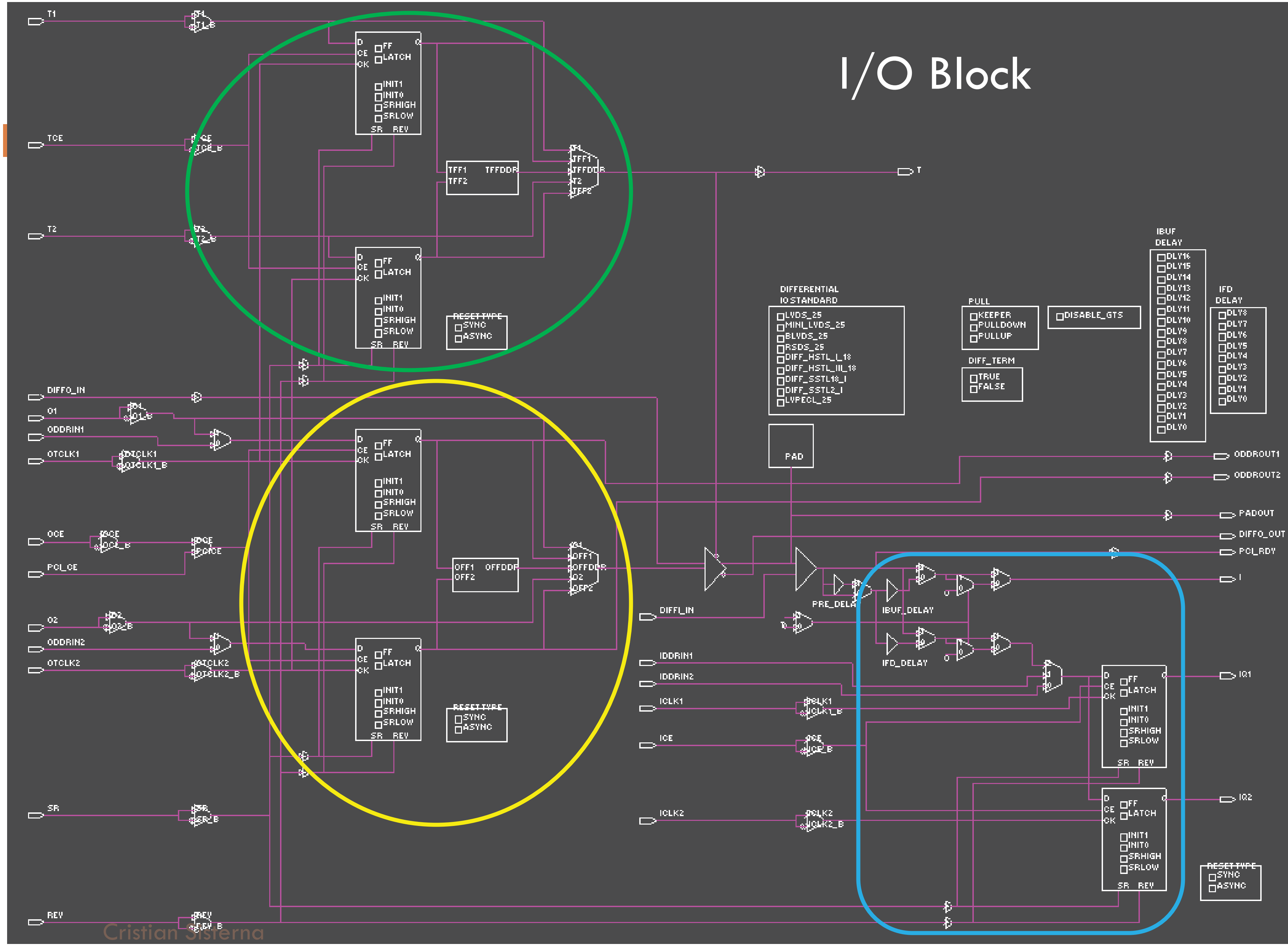

COUT
Reset Type
Sync
Async
DMUX
D
DQ
CMUX
C
CQ
BMUX
B
BQ
AMUX
A
AQ
D6
D5
D4
D3
D2
D1
DX
C6
C5
C4
C3
C2
C1
CX
B6
B5
B4
B3
B2
B1
BX
A6
A5
A4
A3
A2
A1
AX
SR
CE
CLK
A6
A5
A4
A3
A2
A1
LUT
ROM
O6
O5
FF
LATCH
INIT1
INIT0
SRHIGH
SRLOW
D
CE
CK
Q
SR
REV
0/1
CIN
UG190_5_04_032606

I/O Resources

Spartan 3 I/O Block (IOB)

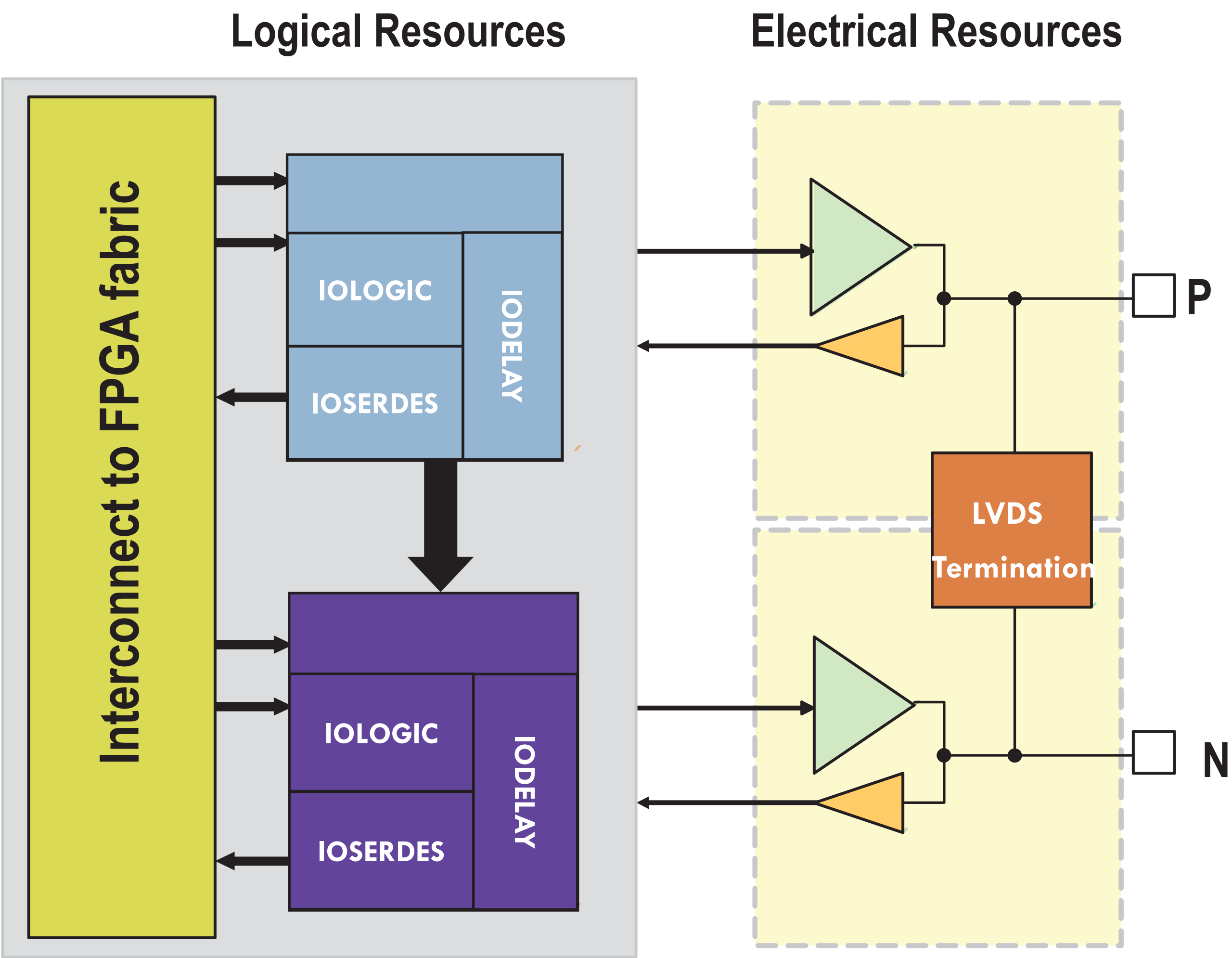


I/O Block



T1
TCE
T2
DIFFO_IN
O1
ODDRIN1
OTCLK1
OCE
PCI_CE
O2
ODDRIN2
OTCLK2
SR
REV
D
CE
CK
FF
LATCH
INIT1
INIT0
SRHIGH
SRLOW
SR
REV
TFF1
TFF2
TFFDDR
RESETTYPE
SYNC
ASYNC
OFF1
OFF2
OFFDDR
T
DIFFERENTIAL
IO STANDARD
LVDS_25
MINI_LVDS_25
BLVDS_25
RSDS_25
DIFF_HSTL_I_18
DIFF_HSTL_III_18
DIFF_SSTL18_I
DIFF_SSTL2_I
LVPECL_25
PULL
KEEPER
PULLDOWN
PULLUP
DISABLE_GTS
DIFF_TERM
TRUE
FALSE
IBUF
DELAY
DLY16
DLY15
DLY14
DLY13
DLY12
DLY11
DLY10
DLY9
DLY8
DLY7
DLY6
DLY5
DLY4
DLY3
DLY2
DLY1
DLY0
IFD
DELAY
PAD
ODDROUT1
ODDROUT2
PADOUT
DIFFO_OUT
PCI_RDY
I
IQ1
IQ2
DIFFI_IN
IDDRIN1
IDDRIN2
ICLK1
ICE
ICLK2
PRE_DELAY
IBUF_DELAY
IFD_DELAY

Spartan 6 I/O Block Diagram



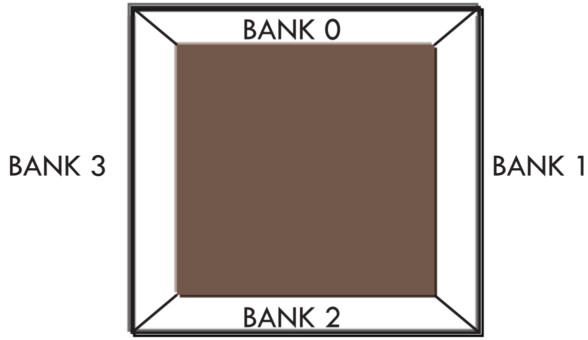
- IOSERDES
  - Parallel to serial converter (serializer)
  - Serial to parallel converter (De-serializer)
- IODELAY
  - Selectable fine-grained delay
- SDR and DDR resources

S6 - FPGA Supports 40+ Standards

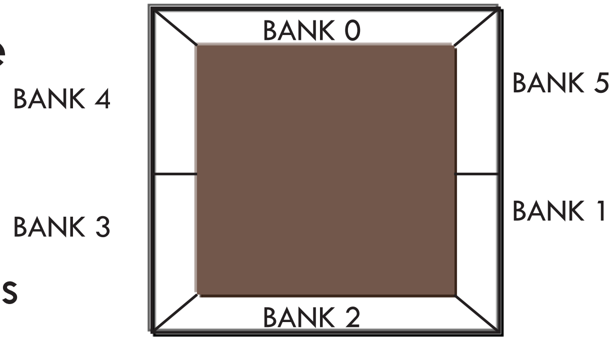
- Each input can be 3.3 V compatible
- LVCMOS (3.3 V, 2.5 V, 1.8 V, 1.5 V, and 1.2 V)
- LVCMOS_JEDEC
- LVPECL (3.3 V, 2.5 V)
- PCI
- **I2C***
- HSTL (1.8 V, 1.5 V; Classes I, II, III, IV)
  - DIFF_HSTL_I, DIFF_HSTL_I_18
  - **DIFF_HSTL_II***
- SSTL (2.5 V, 1.8 V; Classes I, II)
  - DIFF_SSTL_I, DIFF_SSTL18_I
  - **DIFF_SSTL_II***
- LVDS, Bus LVDS
- RSDS_25 (point-to-point)

S6 - FPGA I/O Bank Structure

- All I/Os are on the edges of the chip
- I/Os are grouped into banks
  - 30 ~ 83 I/O per banks
  - Eight clock pins per edge
  - Common VCCO, VREF
    - Restricts mixture of standards in one bank
- The differential driver is only available in
  Bank0 and Bank2
  - Differential receiver is available in all banks
  - On-chip termination is available in all banks



Chip View
(LX45/T and Smaller)



Chip View
(LX100/T and Larger)

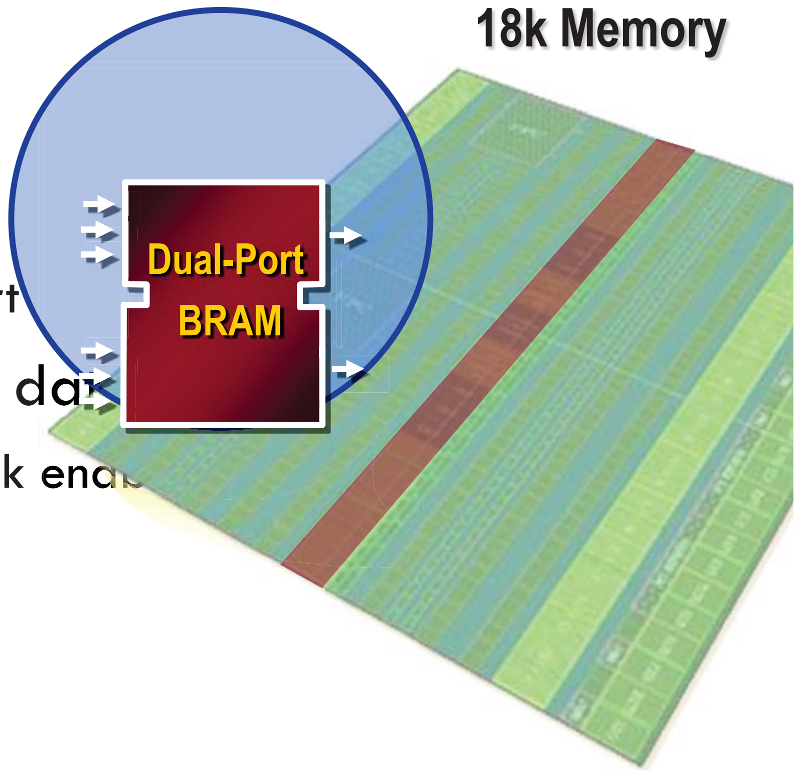
I/O Resources

- Digital Controlled Impedance (DCI)
- Drive Strenght
- Slew Rate
- Bus Hold (Bus keeper)
- Pull-up/Pull-down
- Differential Termination
- IODelay (V5, V6, V7)
  - Fixed
  - Variable

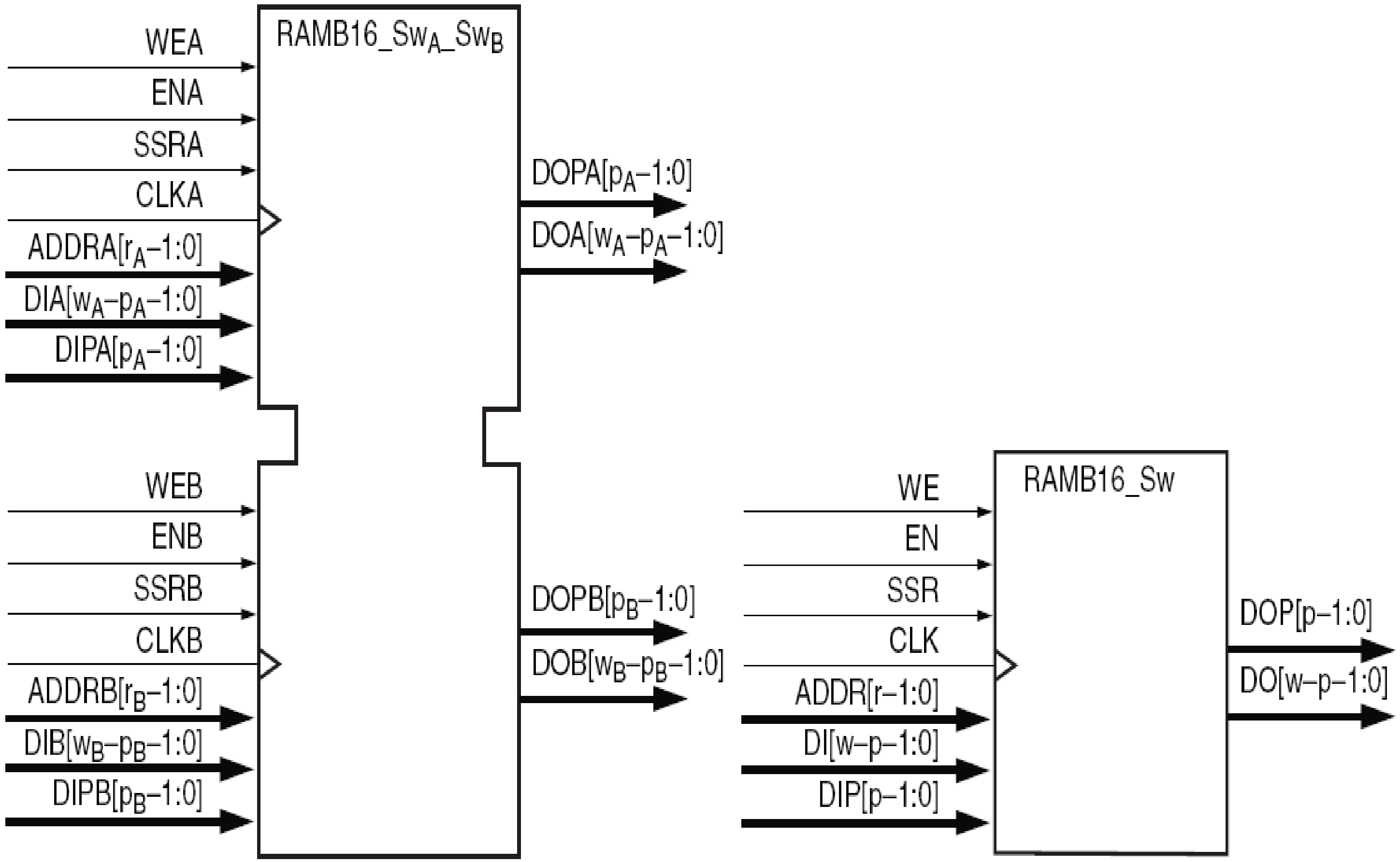
FPGA Memory

FPGA Block RAM (BRAM) Features

- 18 kb size
  - With multiple size configuration
- Multiple configuration options
  - True dual-port, simple dual-port, single-port
- Two independent ports access common da
  - Individual address, clock, write enable, clock ena
  - Independent widths for each port
- Byte-write enable
- Different modes:
  - Write first
  - Read first, then write
  - No change



S3 - Memory Block (BRAM)

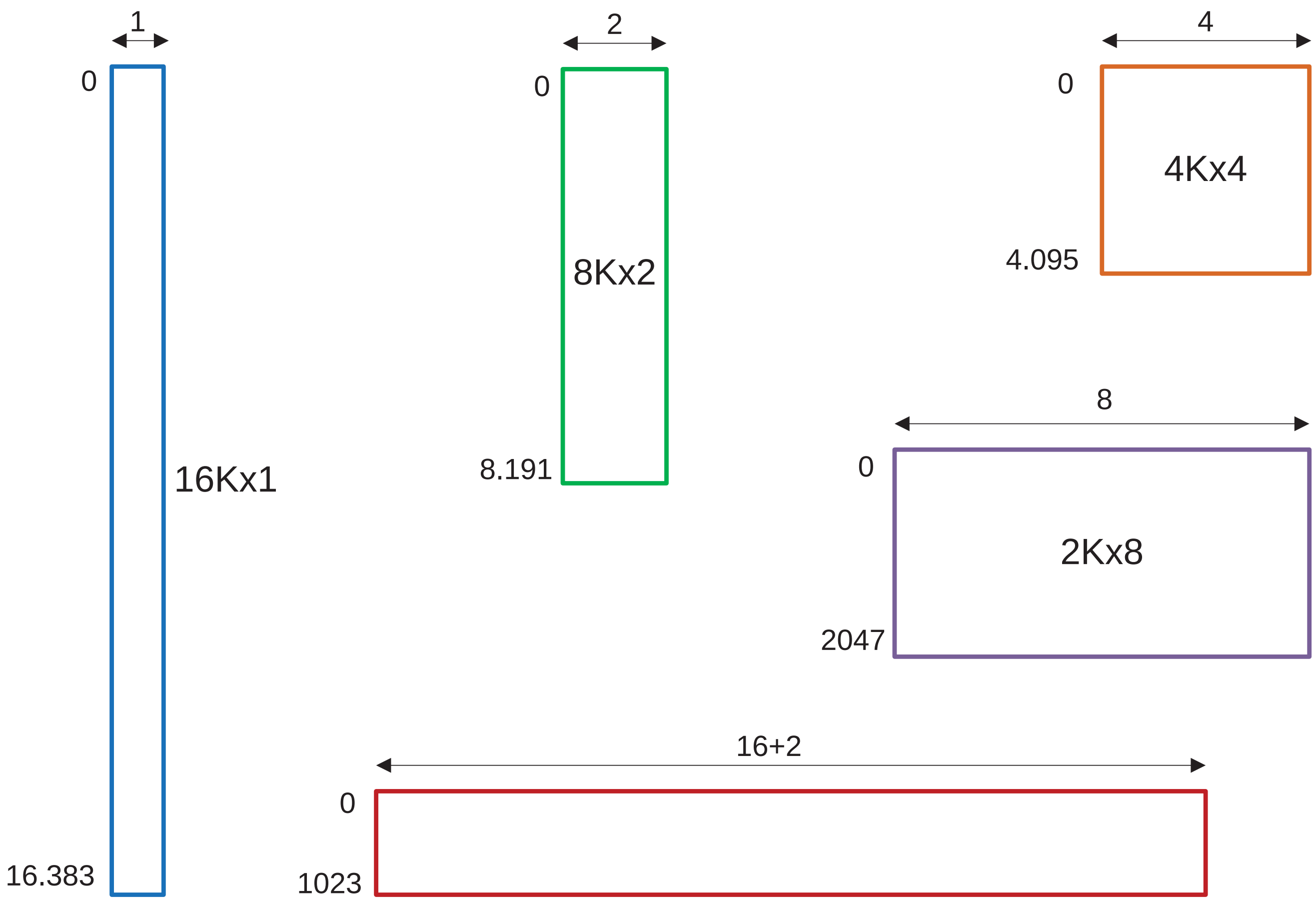


(a) Dual-Port (b) Single-Port

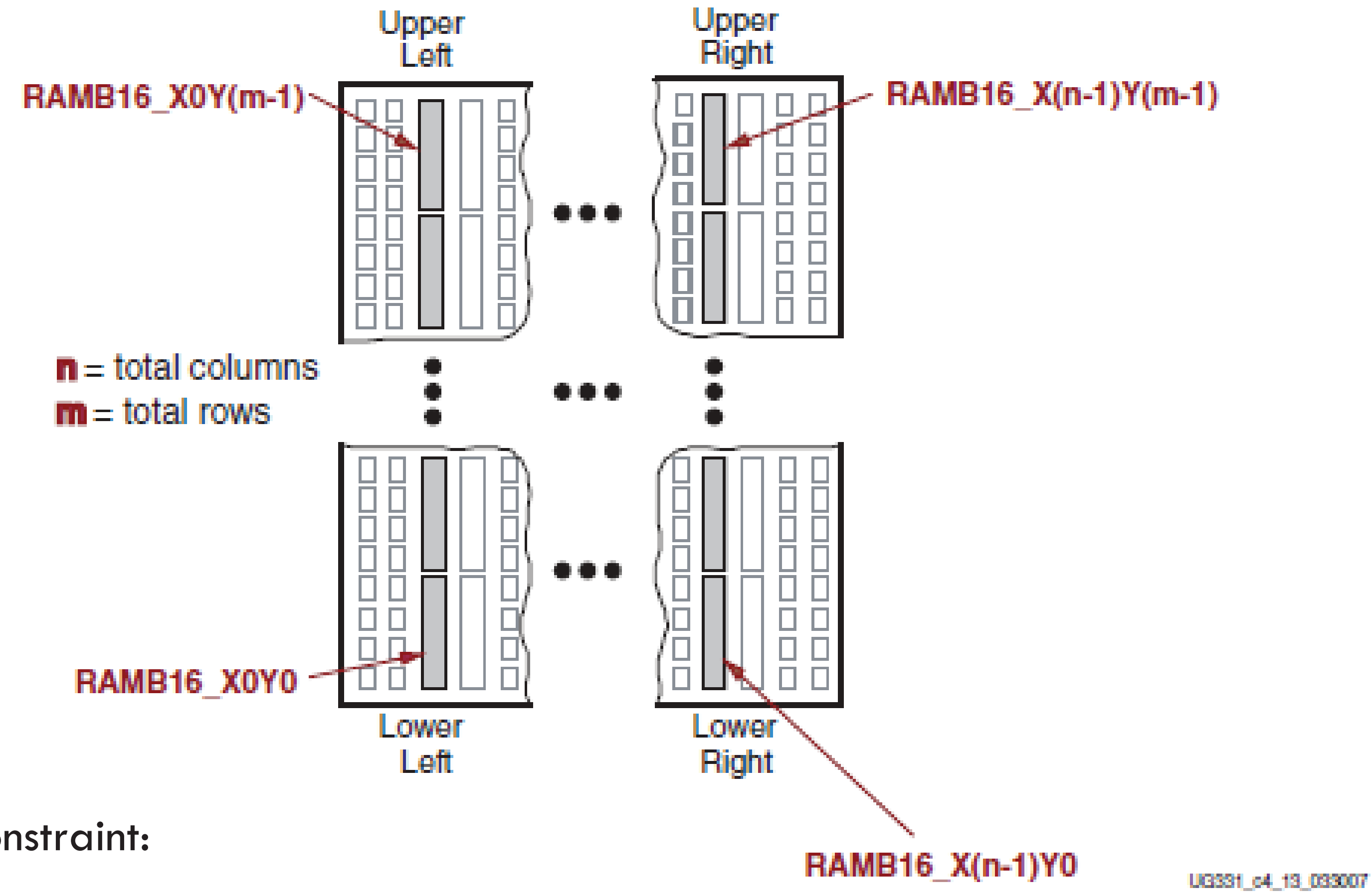
BRAMs Usages

Memories & Storage Elements:			
Asynchronous FIFO	Xilinx	LogiCORE	1-256 bits, 15-65535 words, DRAM or BRAM, independent I/O clock domains
Content Addressable Memory (CAM)	Xilinx	LogiCORE	1-512 bits, 2-10K words, SRL16
Distributed Memory	Xilinx	LogiCORE	1-1024 bit, 16-65536 word, RAM/ROM/SRL16, opt output regs and pipelining
Dual-Port Block Memory	Xilinx	LogiCORE	1-256 bits, 2-13K words
Single-Port Block Memory	Xilinx	LogiCORE	1-256 bits, 2-128K words
Synchronous FIFO	Xilinx	LogiCORE	1-256 bits, 16-256 words, distributed/block RAM

BRAM Configuration Size



BRAM Forced Location



Location Constraint:

LOC <instance> = RAMB16_X#Y#

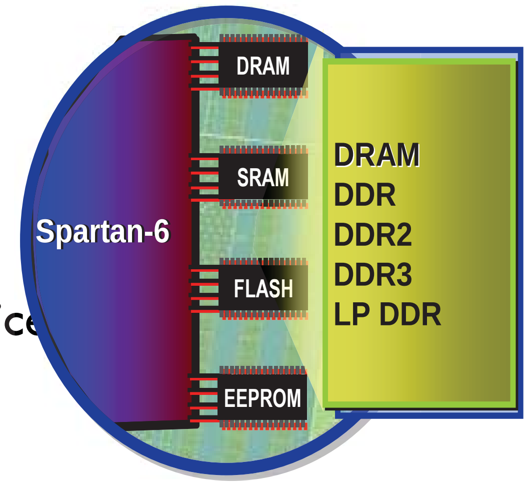
SLICEM Used as Distributed SelectRAM Memory

Single Port	Dual Port	Simple Dual Port	Quad Port
32x2	32x2**D**	32x6**SDP**	32x2**Q**
32x4	32x4**D**	64x3**SDP**	64x1**Q**
32x6	64x1**D**		
32x8	64x2**D**		
64x1	128x1**D**		
64x2			
64x3			
64x4			
128x1			
128x2			
256x1			

- Uses the same storage that is used for the look-up table function
- Synchronous write, asynchronous read
  - Can be converted to synchronous read using the flip-flops available in the slice
- Various configurations
  - Single port
    - One LUT6 = 64x1 or 32x2 RAM
    - Cascadable up to 256x1 RAM
  - Dual port (**D**)
    - 1 read / write port + 1 read-only port
  - Simple dual port (**SDP**)
    - 1 write-only port + 1 read-only port
  - Quad-port (**Q**)
    - 1 read / write port + 3 read-only ports

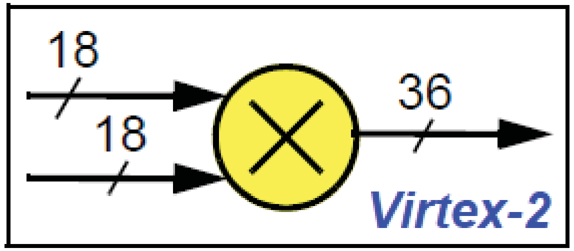
S6 - Memory Controller

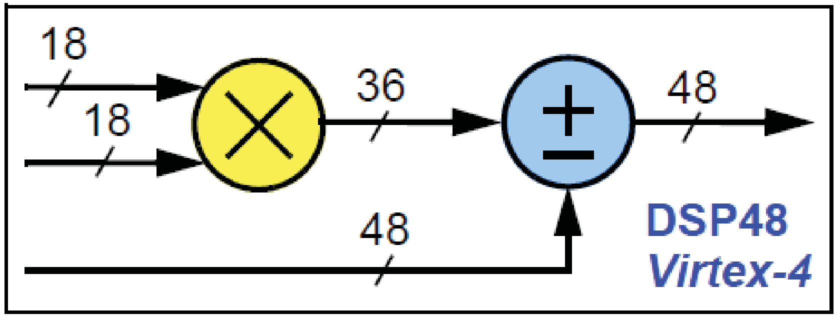
- Only low cost FPGA with a "hard" memory controller
- Guaranteed memory interface performance providing
  - Reduced engineering & board design time
  - DDR, DDR2, DDR3 & LP DDR support
  - Up to 12.8Mbps bandwidth for each memory controller
- Automatic calibration features
- Multiport structure for user interface
  - Six 32-bit programmable ports from fabric
  - Controller interface to 4, 8 or 16 bit memories devic

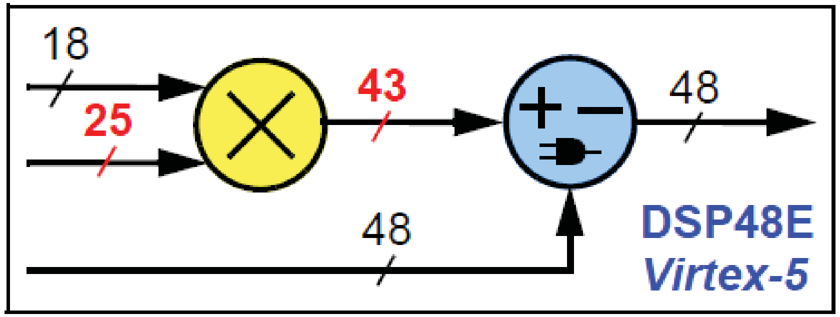


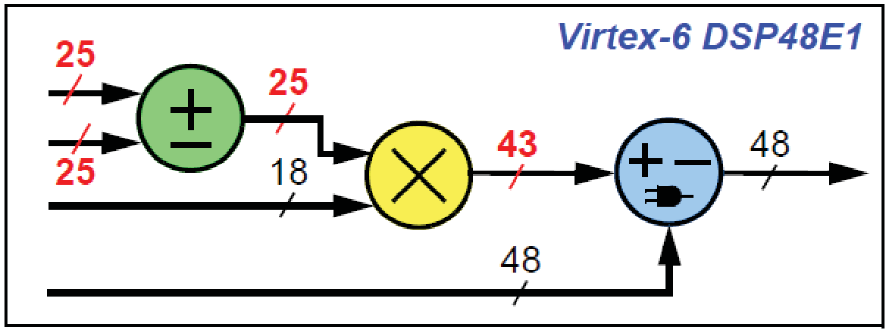
FPGA Multipliers and DSP Blocks

Different Multipliers/DSP Blocks

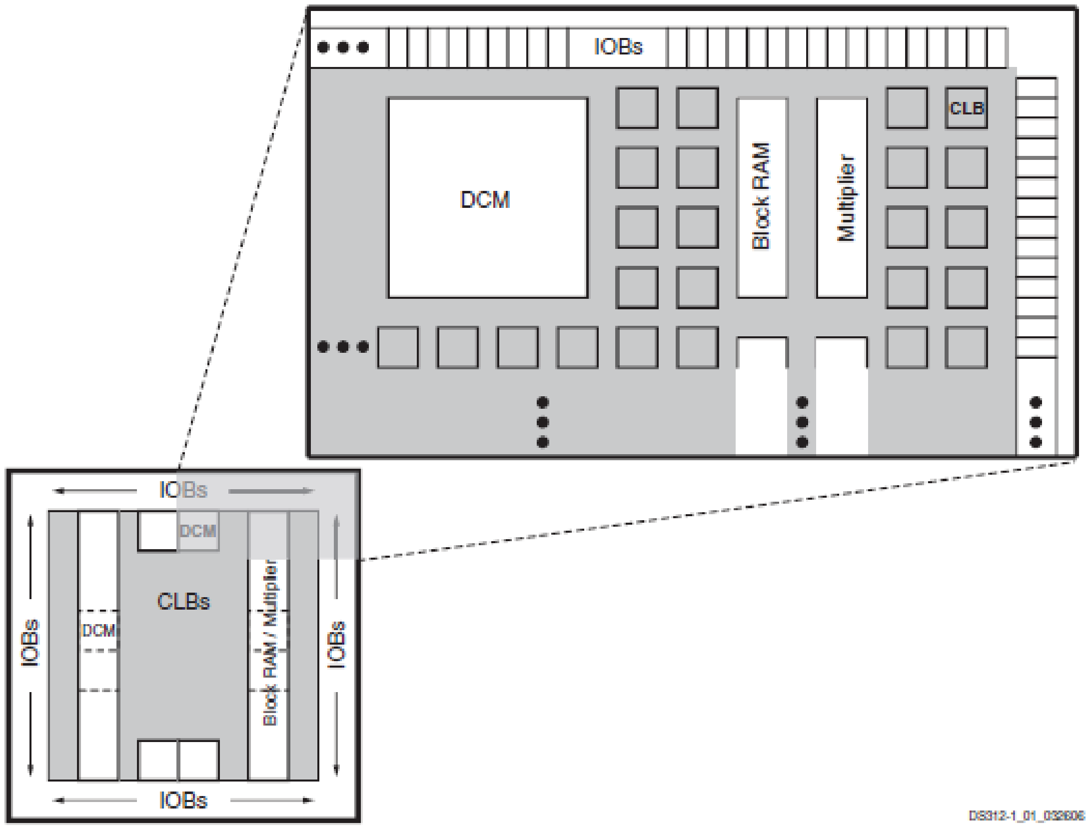




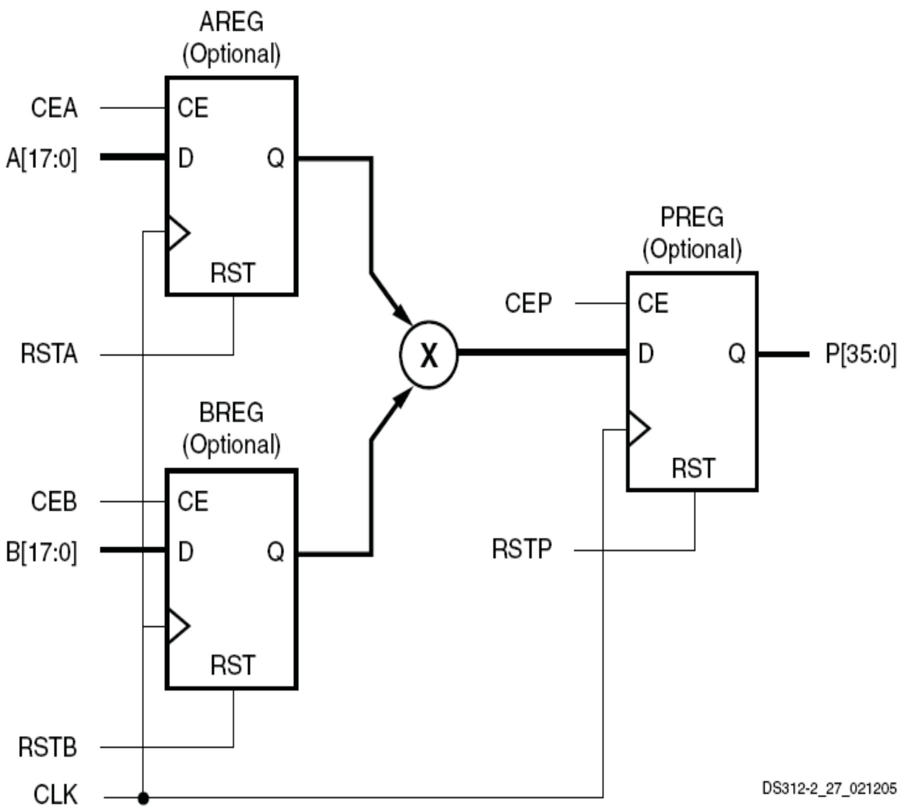




S3 – Multiplier Locations



Spartan 3 - Multiplier

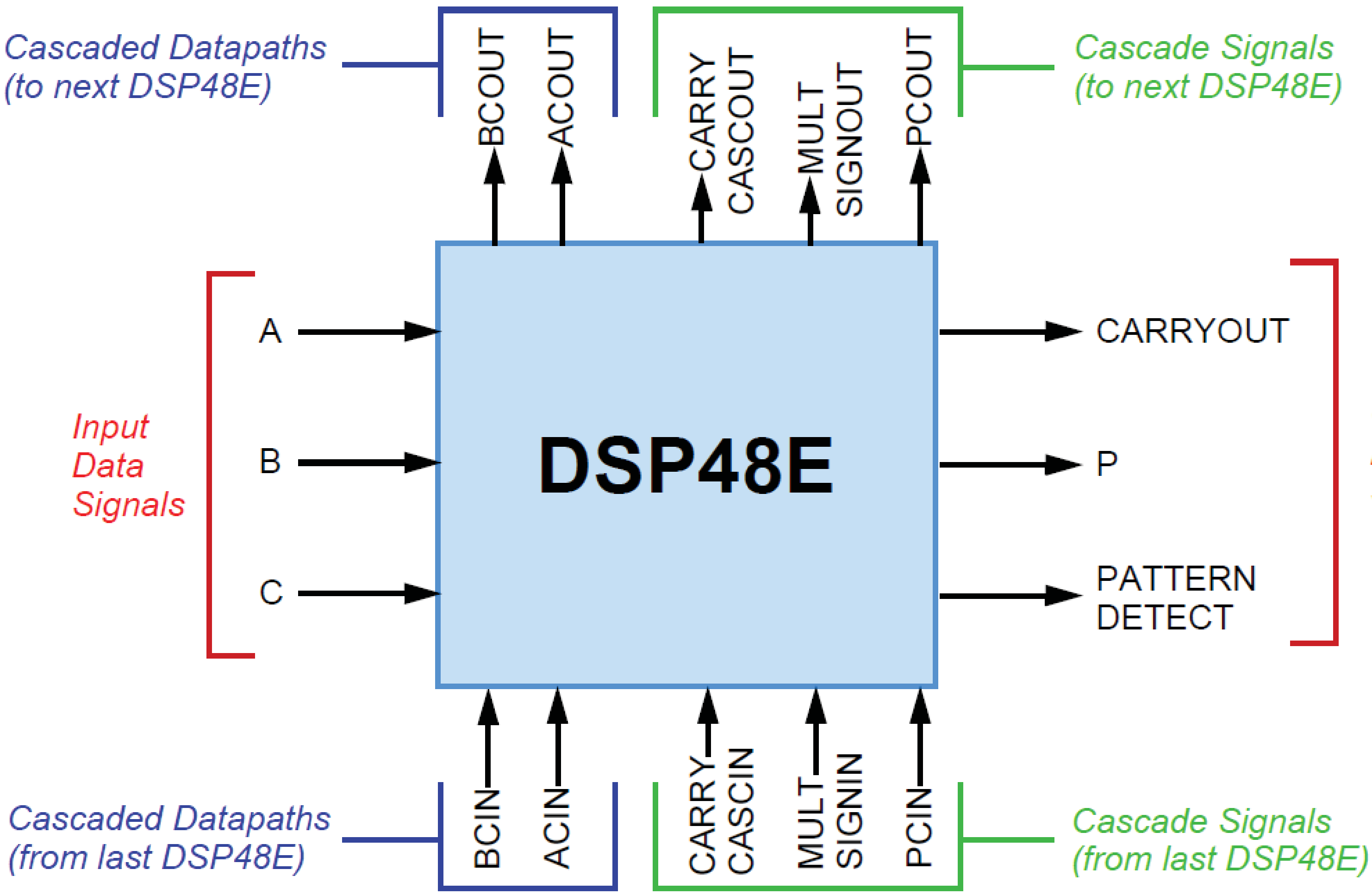


P = A x B

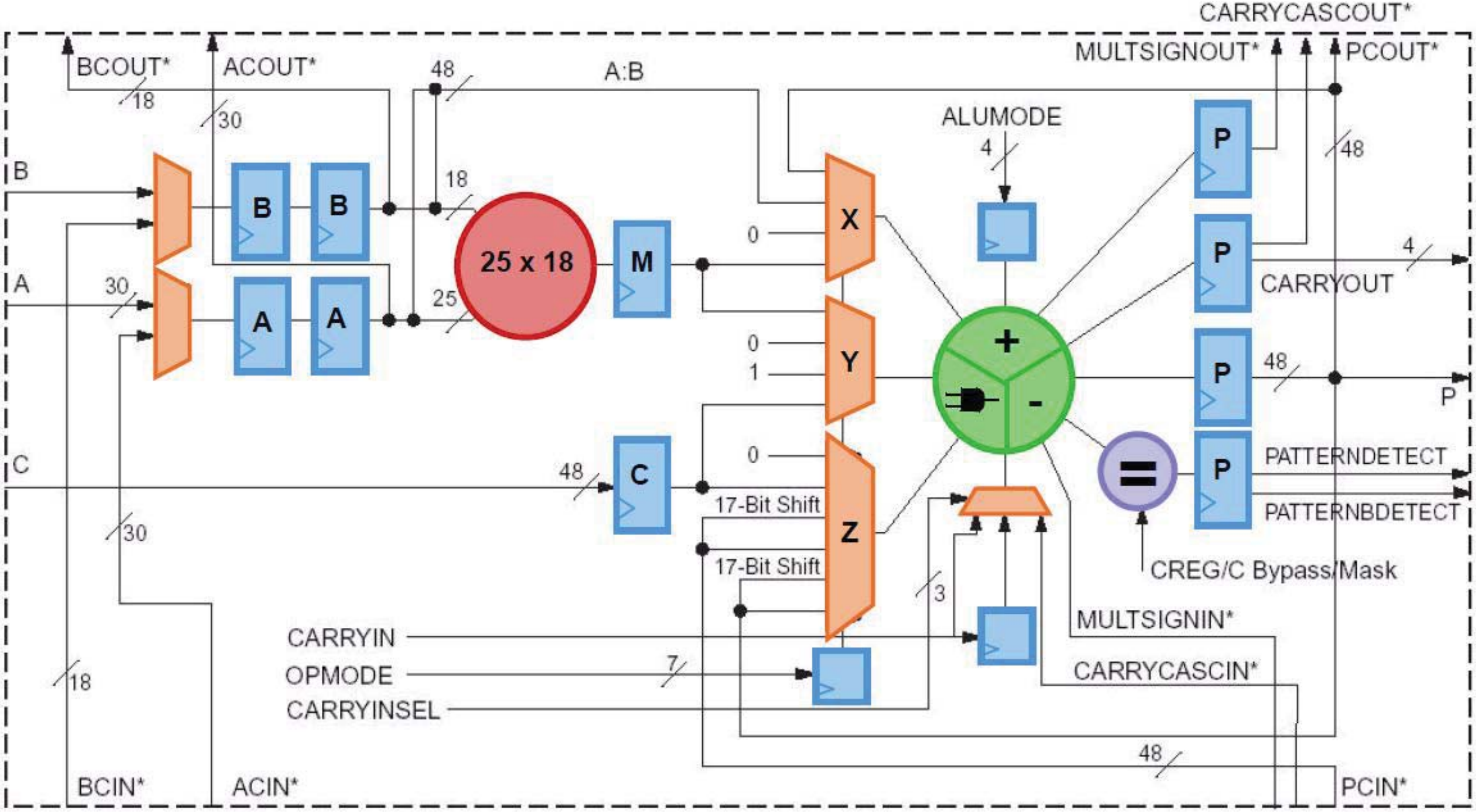
36 = 18 x 18

Pipelining (optional)

Virtex 5/6 - Conexiones del DSP48E

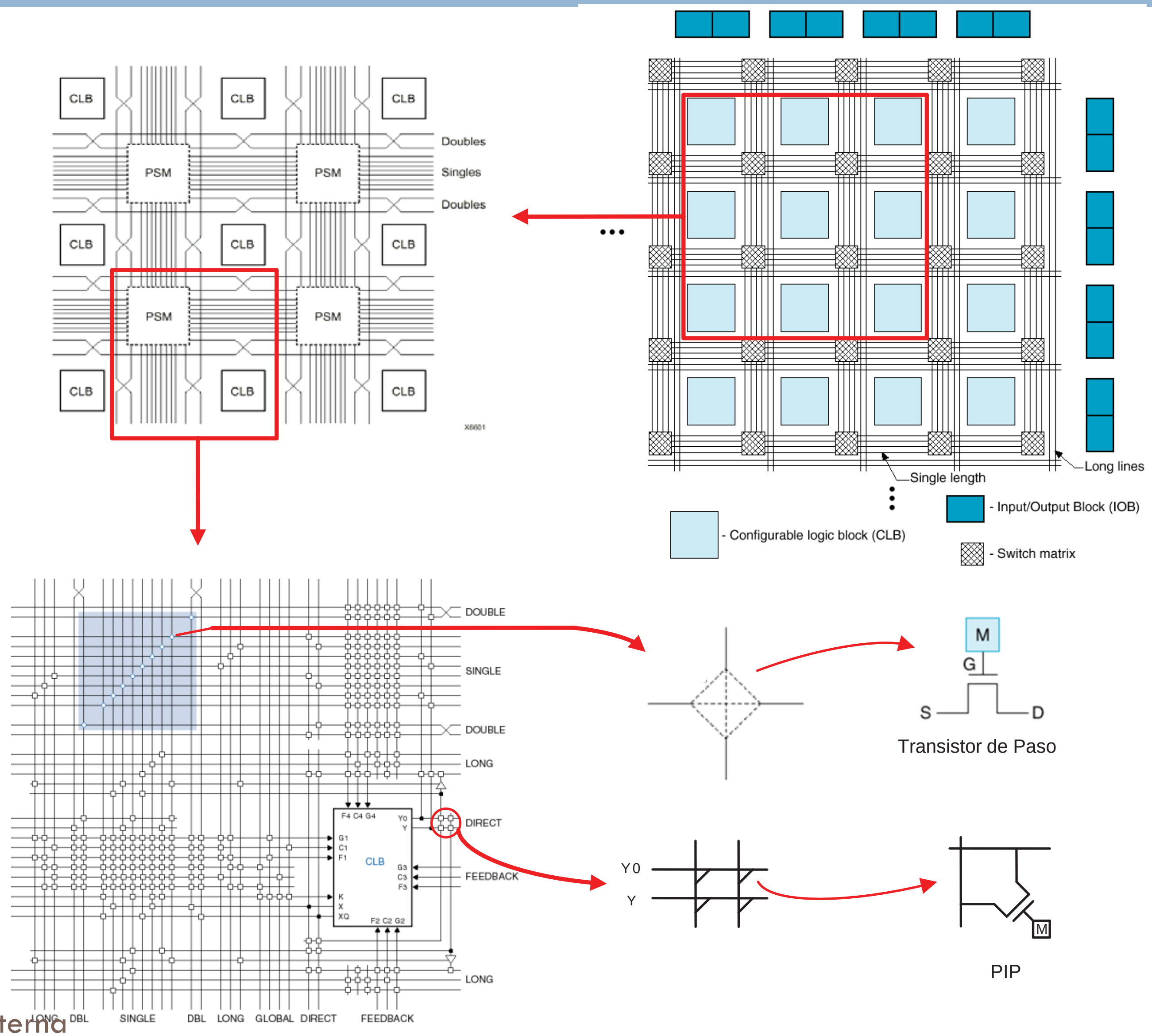


Virtex 5/6 - Bloque DSP48E



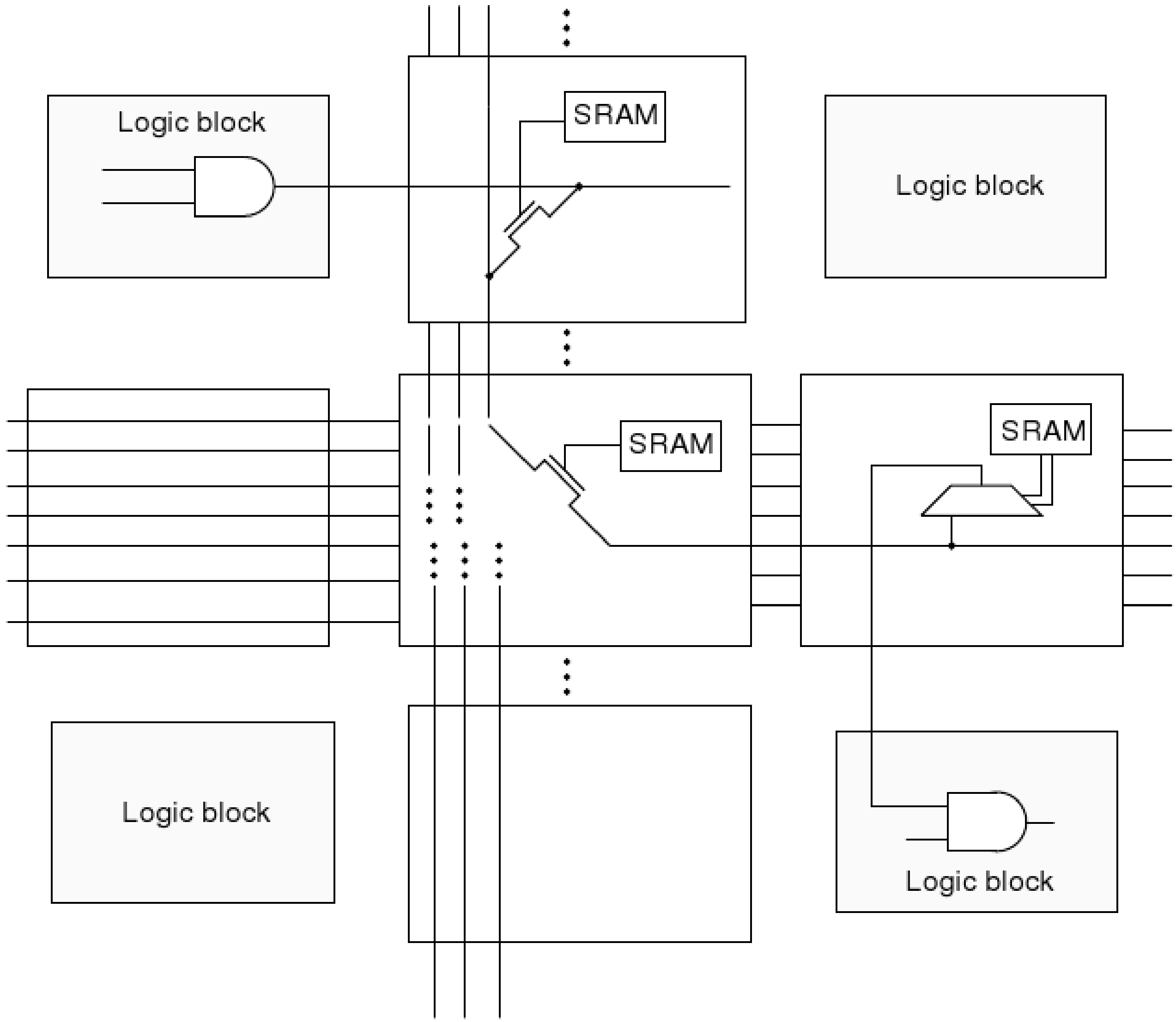
FPGA Routing

Routing



CLB
PSM
Doubles
Singles
Doubles
X6601
Single length
Long lines
- Input/Output Block (IOB)
- Configurable logic block (CLB)
- Switch matrix
DOUBLE
SINGLE
DOUBLE
LONG
DIRECT
FEEDBACK
LONG
LONG DBL SINGLE DBL LONG GLOBAL DIRECT FEEDBACK
M
G
S
D
Transistor de Paso
Y0
Y
M
PIP

Routing (cont.)

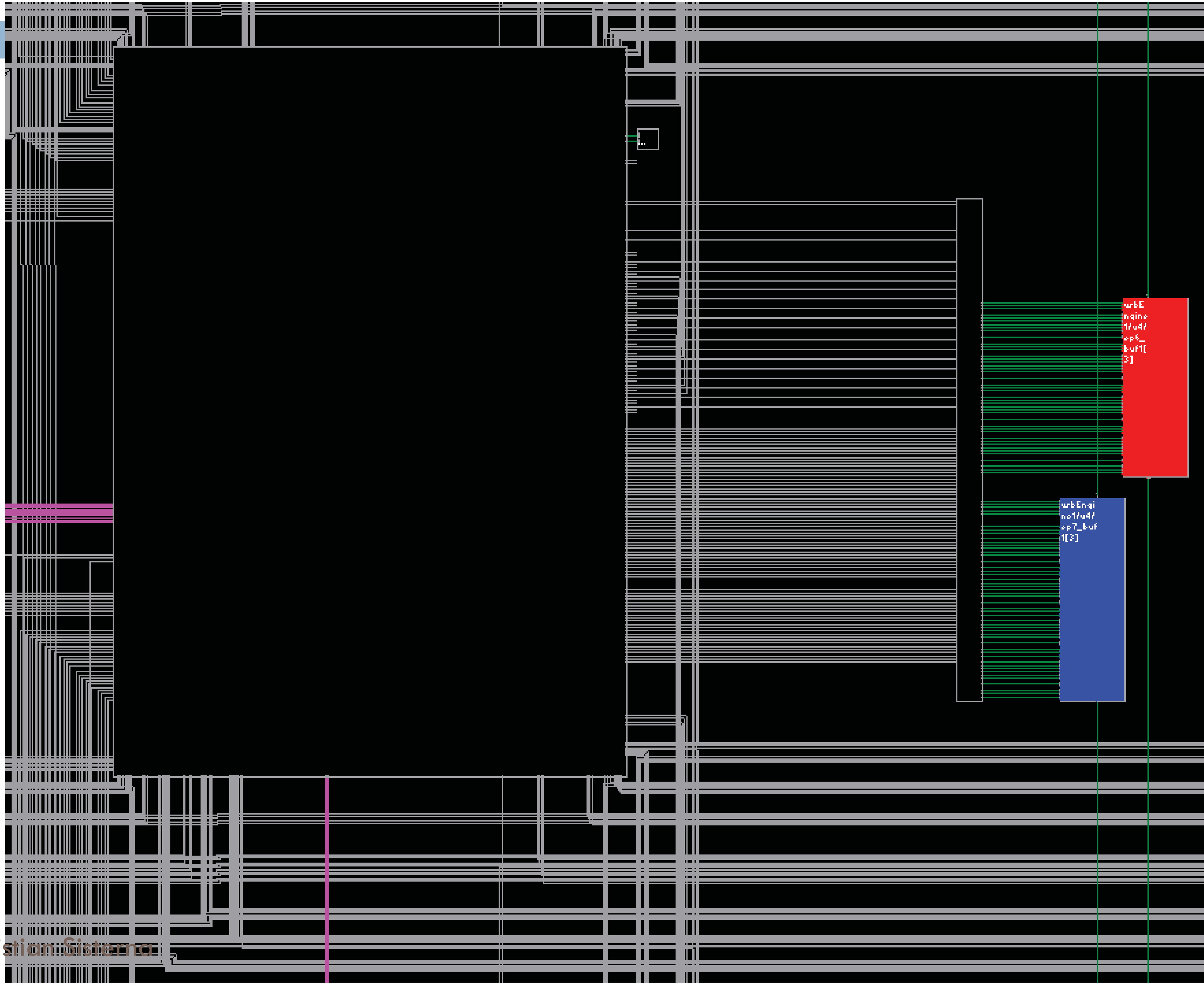


Routing Delay Report

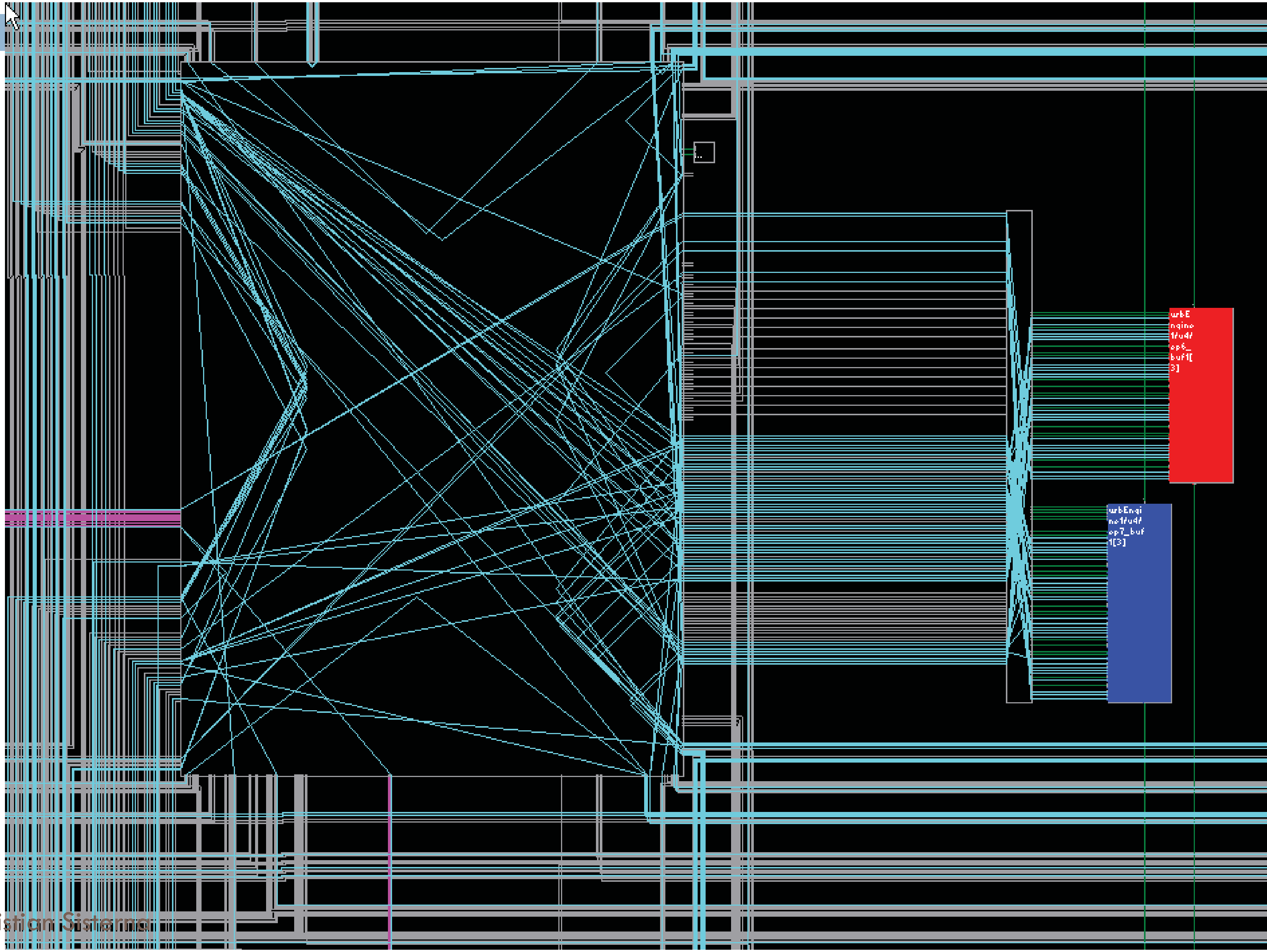

```
--------------------------------------------------------------------------------
Slack:                  0.036ns (requirement - (data path - clock path skew + uncertainty))
  Source:               inst_mem_wrc/c1/BU2/U0/q_i_11 (FF)
  Destination:          inst_mem_wrc/c1/BU2/U0/q_i_12 (FF)
  Requirement:          4.000ns
  Data Path Delay:      3.964ns (Levels of Logic = 3)
  Clock Path Skew:      0.000ns
  Source Clock:         fpga_clk_250 rising at 0.000ns
  Destination Clock:    fpga_clk_250 rising at 4.000ns
  Clock Uncertainty:    0.000ns

  Data Path: inst_mem_wrc/c1/BU2/U0/q_i_11 to inst_mem_wrc/c1/BU2/U0/q_i_12
    Delay type         Delay(ns)  Logical Resource(s)
    ----------------------------  -------------------
    Tcko                  0.374   inst_mem_wrc/c1/BU2/U0/q_i_11
    net (fanout=46)       0.910   addr_wr_i<11>
    Tilo                  0.313   inst_mem_wrc/c1/BU2/U0/thresh0_i_cmp_eq000045
    net (fanout=1)        0.260   inst_mem_wrc/c1/BU2/U0/thresh0_i_cmp_eq000045
    Tilo                  0.313   inst_mem_wrc/c1/BU2/U0/thresh0_i_cmp_eq000059
    net (fanout=2)        0.053   inst_mem_wrc/c1/BU2/U0/thresh0_i
    Tilo                  0.288   inst_mem_wrc/c1/BU2/U0/q_i_or00001
    net (fanout=8)        0.870   inst_mem_wrc/c1/BU2/U0/q_i_or0000
    Tsrck                 0.583   inst_mem_wrc/c1/BU2/U0/q_i_12
    ----------------------------  ---------------------------
    Total                 3.964ns (1.871ns logic, 2.093ns route)
                                  (47.2% logic, 52.8% route)
```

Routing (cont.)

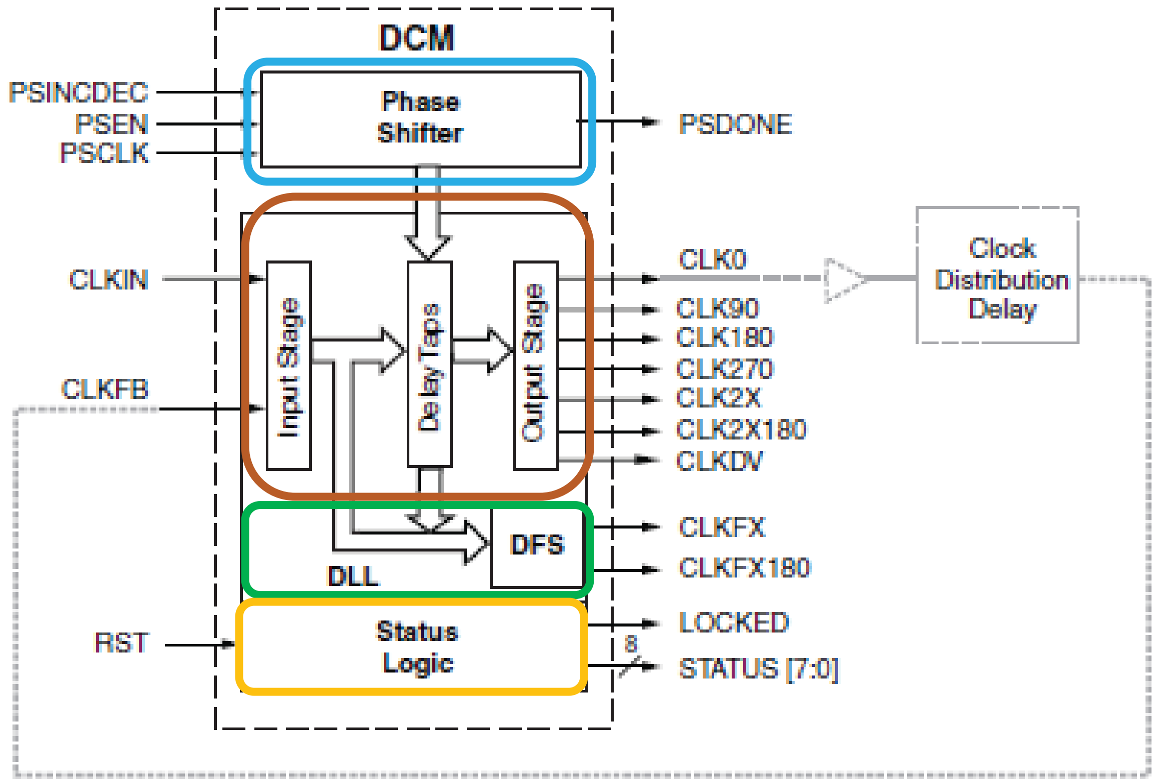


Routing (cont.)

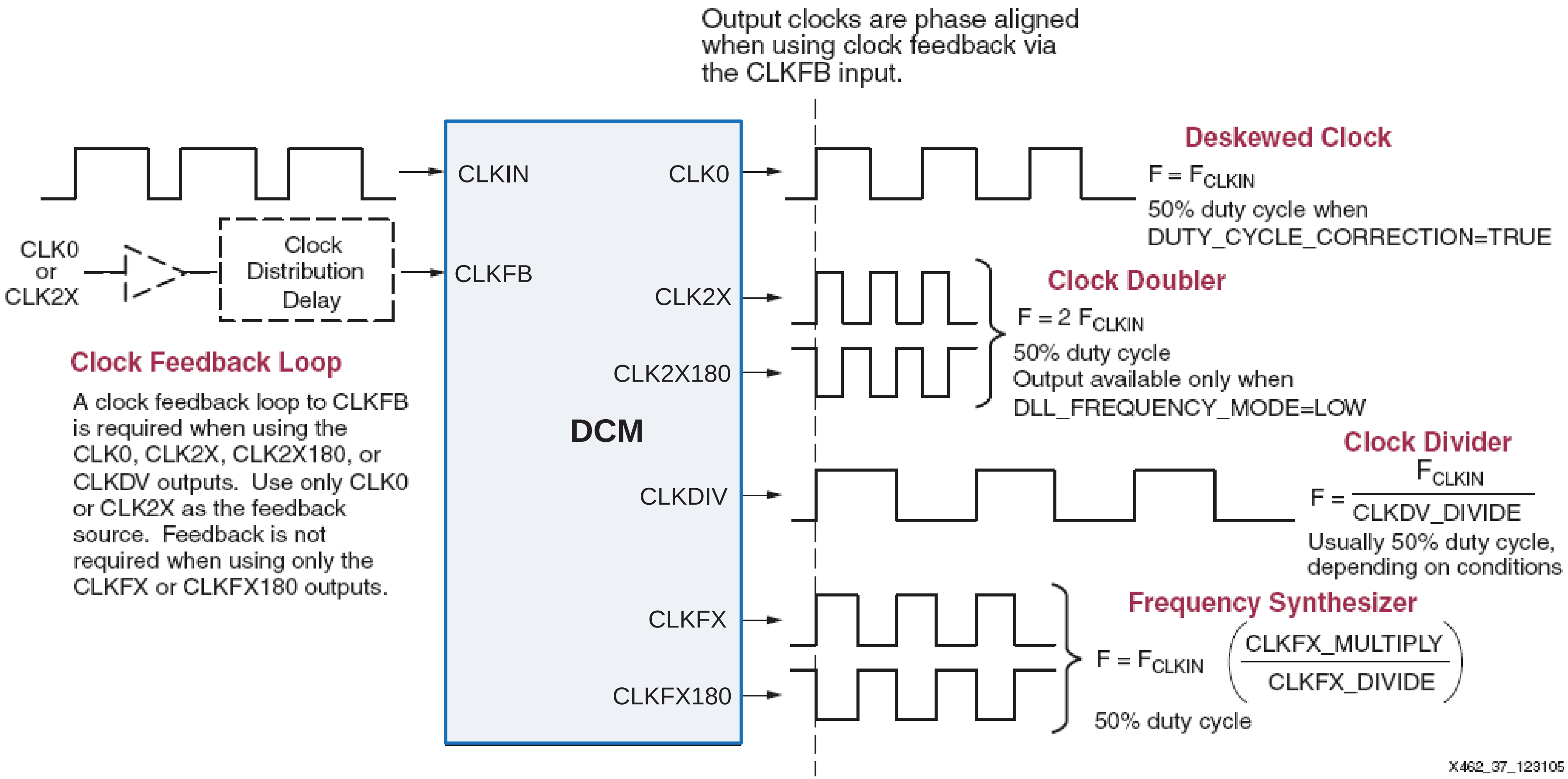


Clock Resources

S3 – Digital Clock Manager



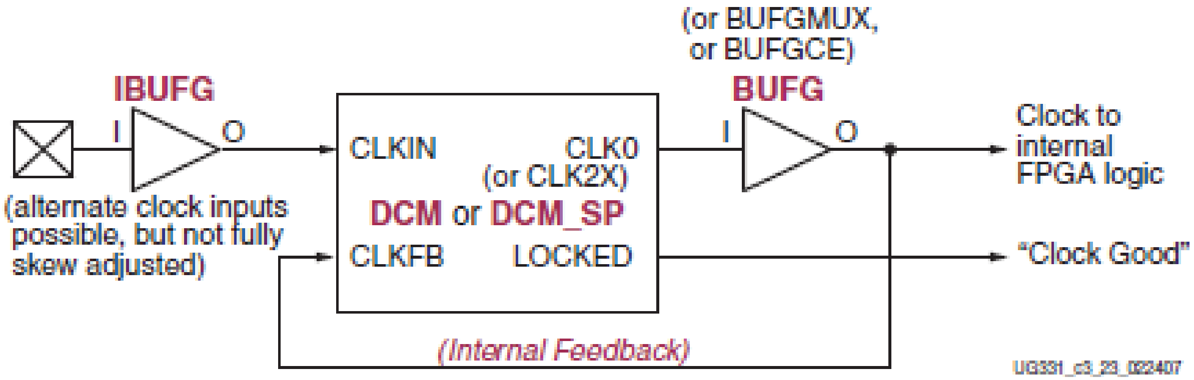
S3 – Digital Clock Manager (cont.)



DCM Purposes

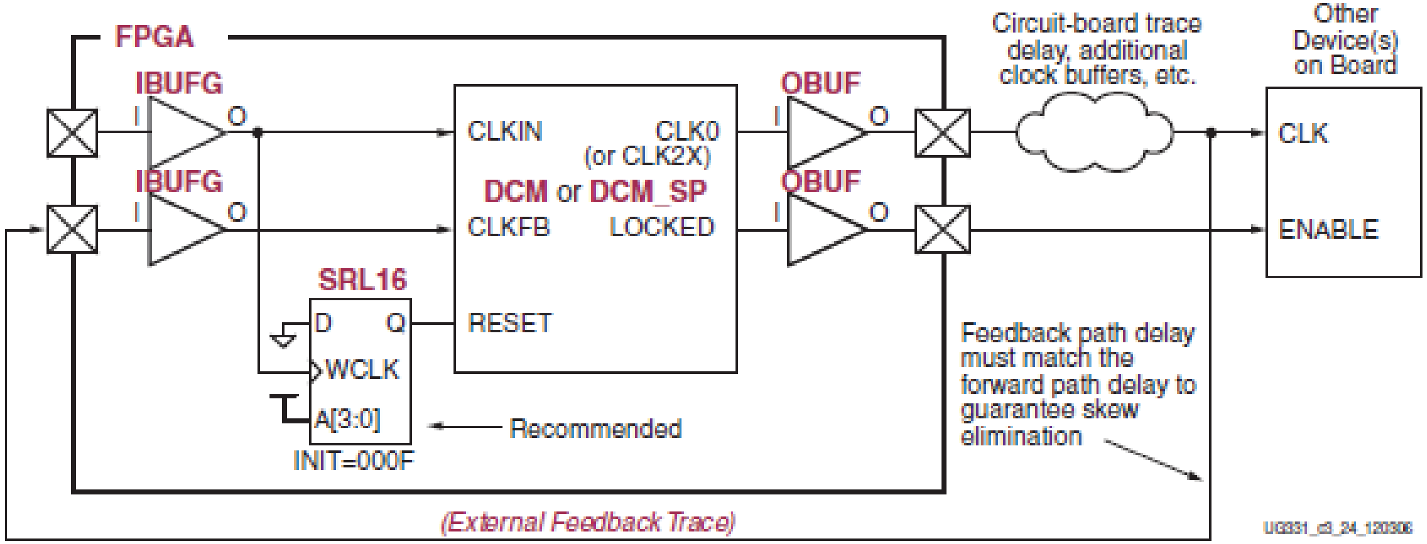
- Elimintating clock skew
- Clock phase shifting
  - Variable
  - Fixed
- Multiply and Divide input clock, to generate a new frequency
- Duty cycle 50%
- Rebuffer clock input

DCM Aplication

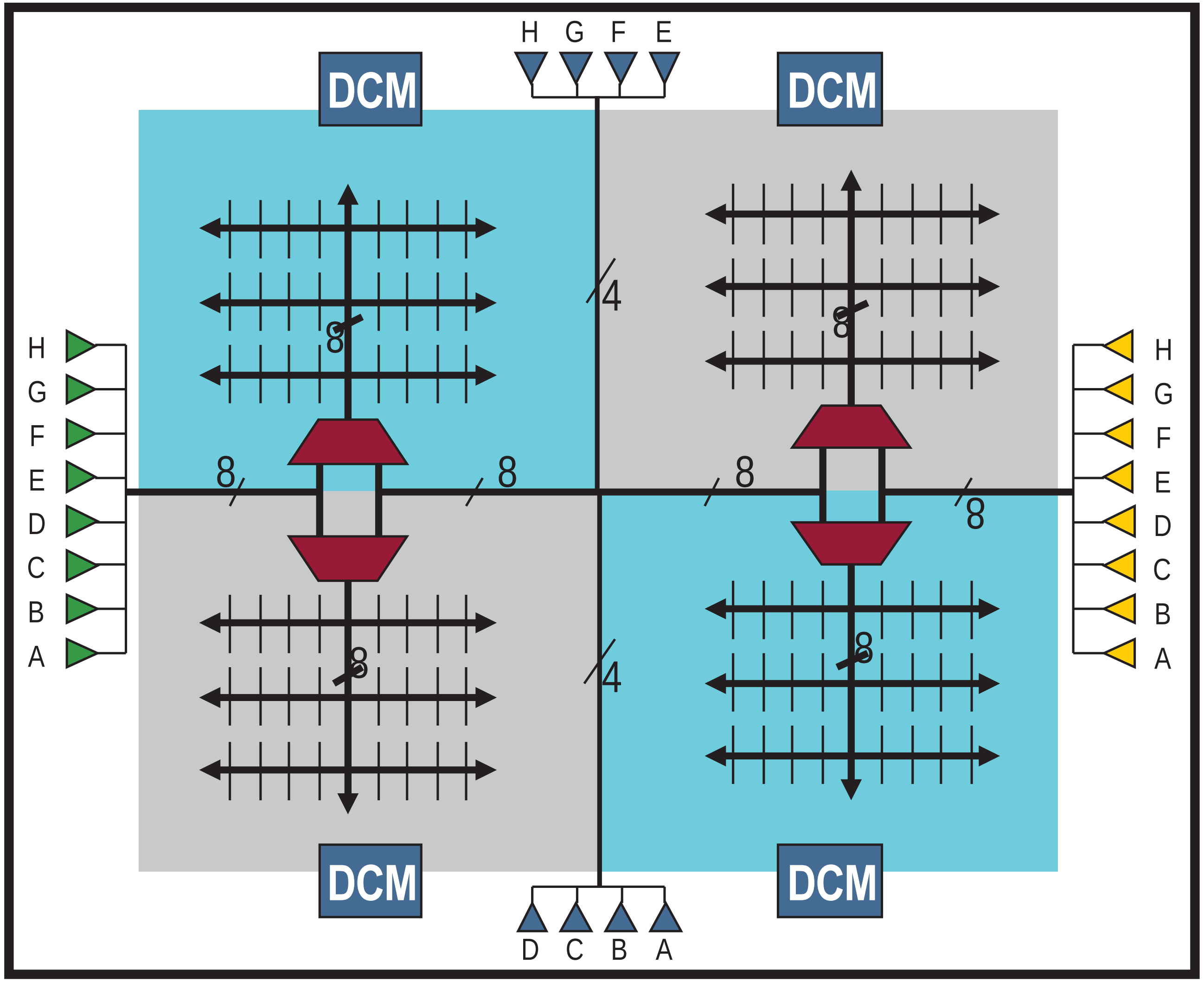


Skew elimination on internal clock signals

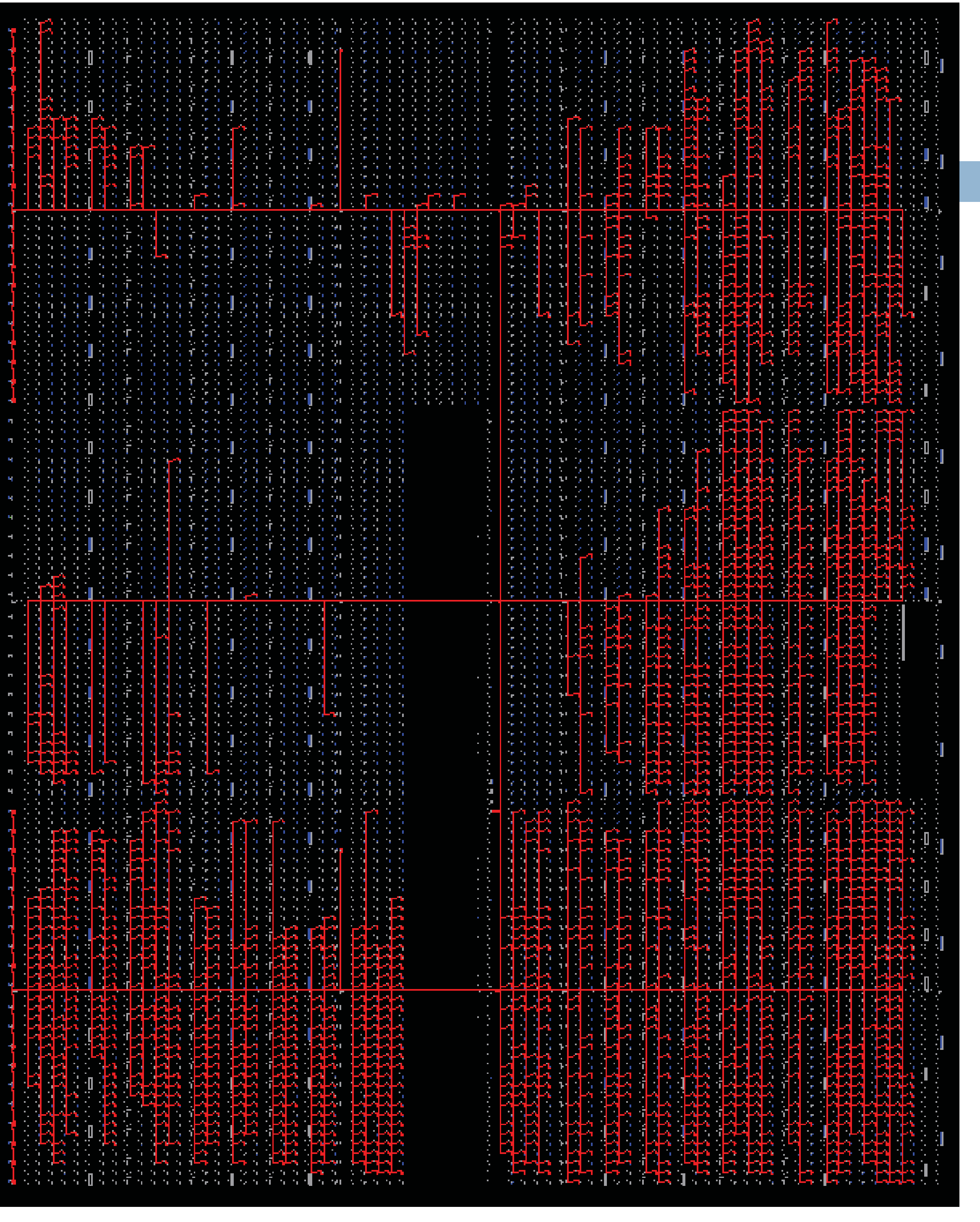
Skew elimination on external clock signal



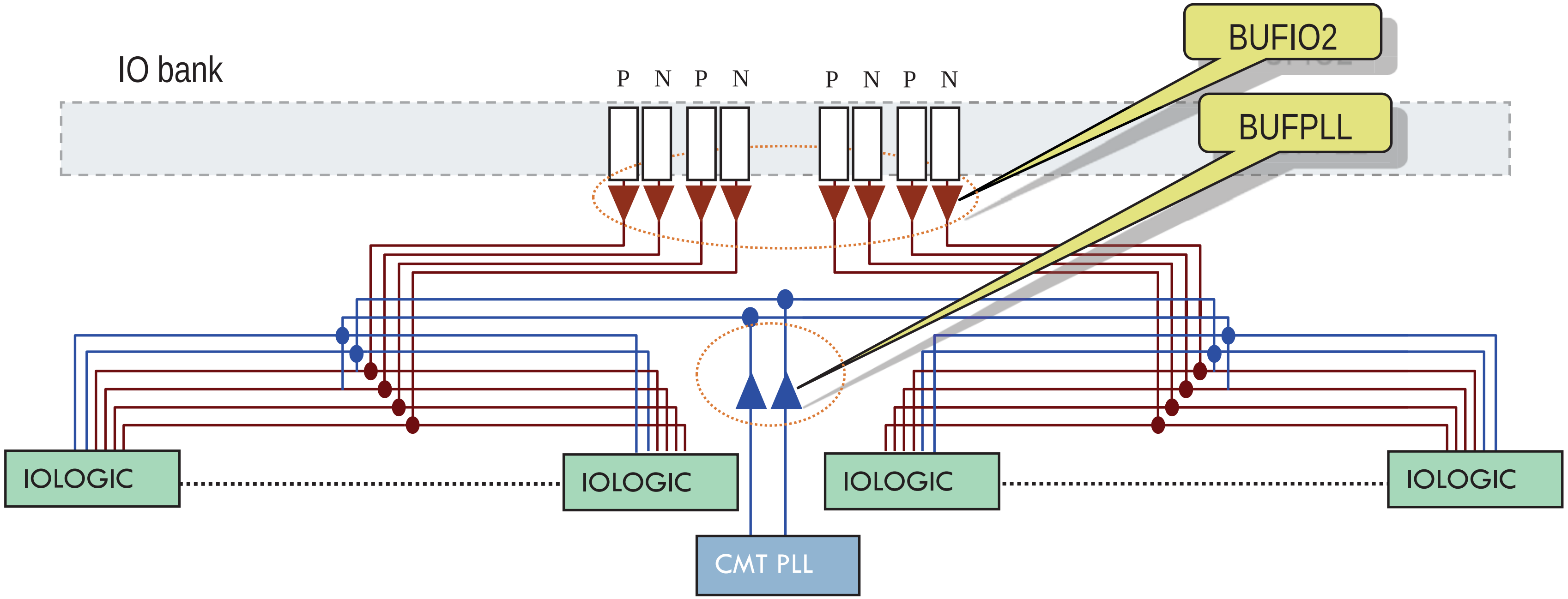
Dedicated Clokc Routing



Dedicated Clock Routing: Real application

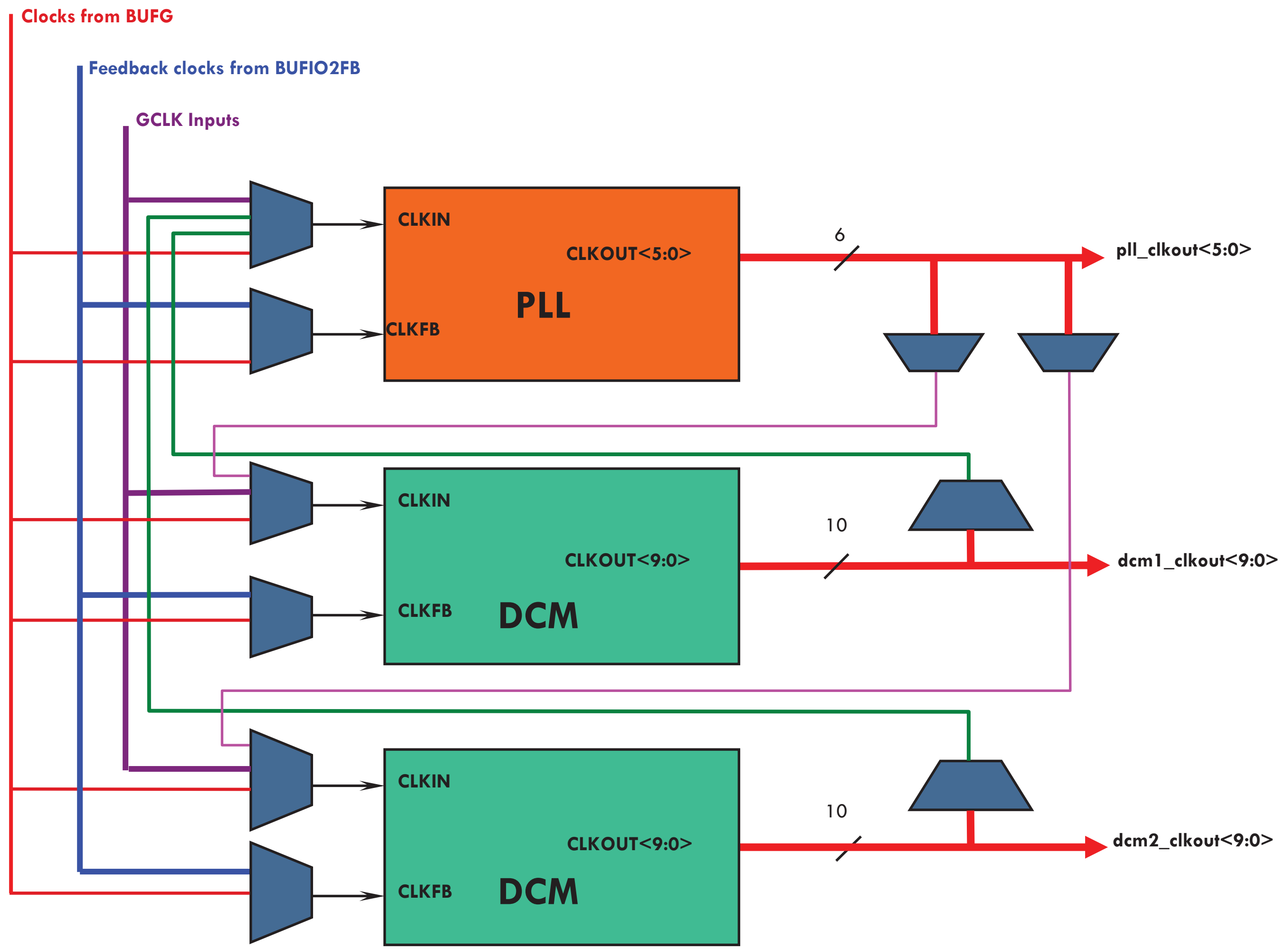


Spartan-6 FPGA I/O Clock Network



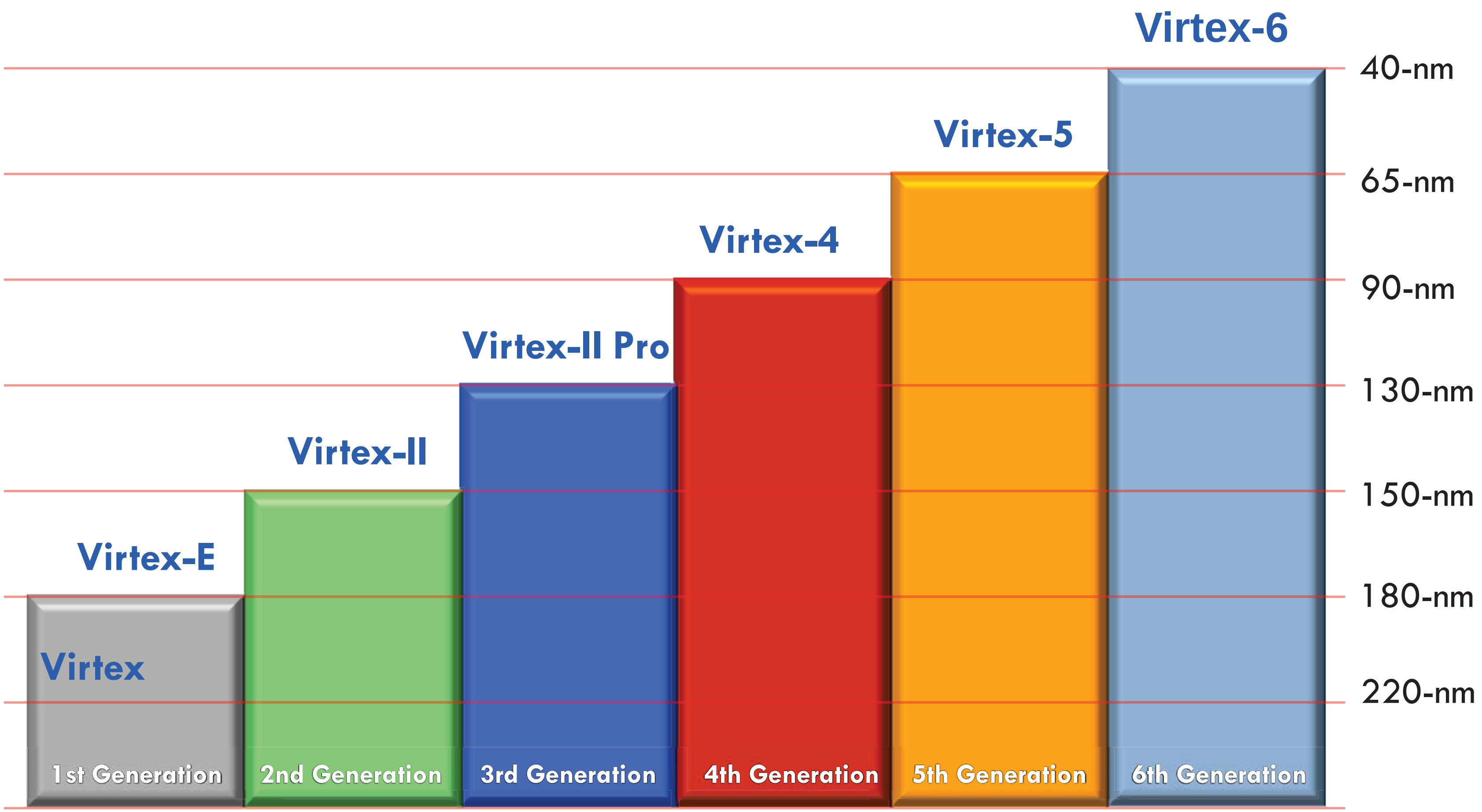
- Special clock network dedicated to I/O logical resources
  - Independent of global clock resources
  - Speeds up to 1 GHz
- Multiple sources for clocking I/O logic
  - BUFIO2: for high-speed dedicated I/O clock signals
  - BUFPLL: for clocks driven by the PLL in the CMT

Spartan-6 FPGA Clock Management Tile (CMT)

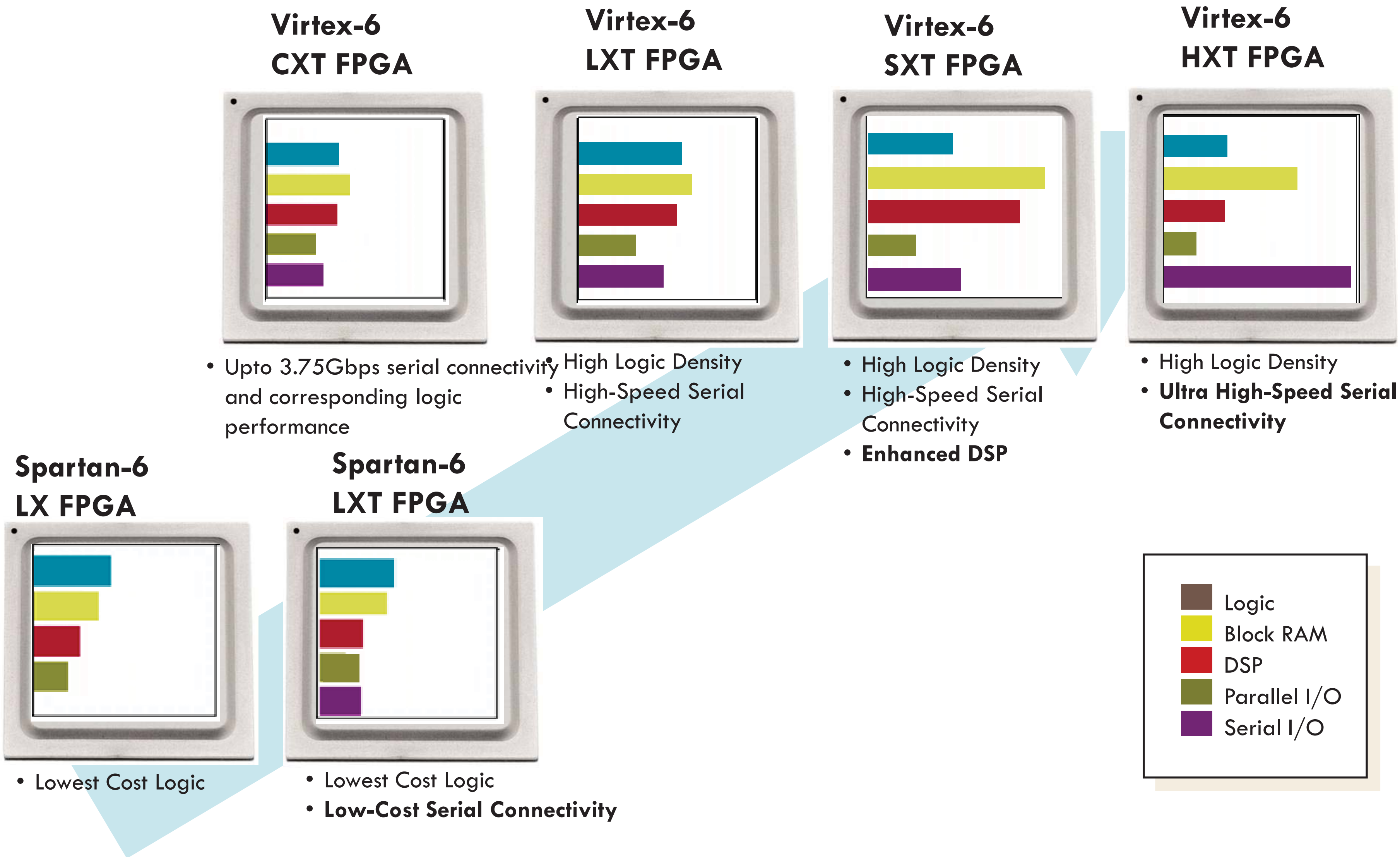


Spartan 6 - Virtex 6 - Virtex 7

Virtex® Product & Process Evolution



Virtex-6 and Spartan-6 FPGA Sub-Families



Virtex 7

- Common elements enable easy IP reuse for quick design portability across all 7 series families
  - Design scalability from low-cost to high-performance
  - Expanded eco-system support
  - Quickest TTM

Logic Fabric
LUT-6 CLB

Precise, Low Jitter Clocking
MMCMs

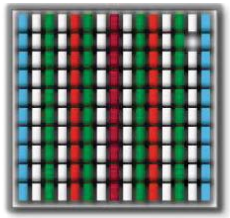
On-Chip Memory
36Kbit/18Kbit Block RAM

Enhanced Connectivity
PCIe® Interface Blocks

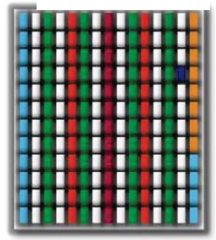
DSP Engines
DSP48E1 Slices

Hi-perf. Parallel I/O Connectivity
SelectIO™ Technology

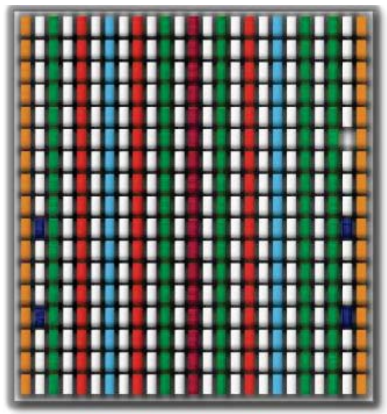
Hi-performance Serial I//O Connectivity
Transceiver Technology



Artix™-7 FPGA



Kintex™-7 FPGA



Virtex®-7 FPGA

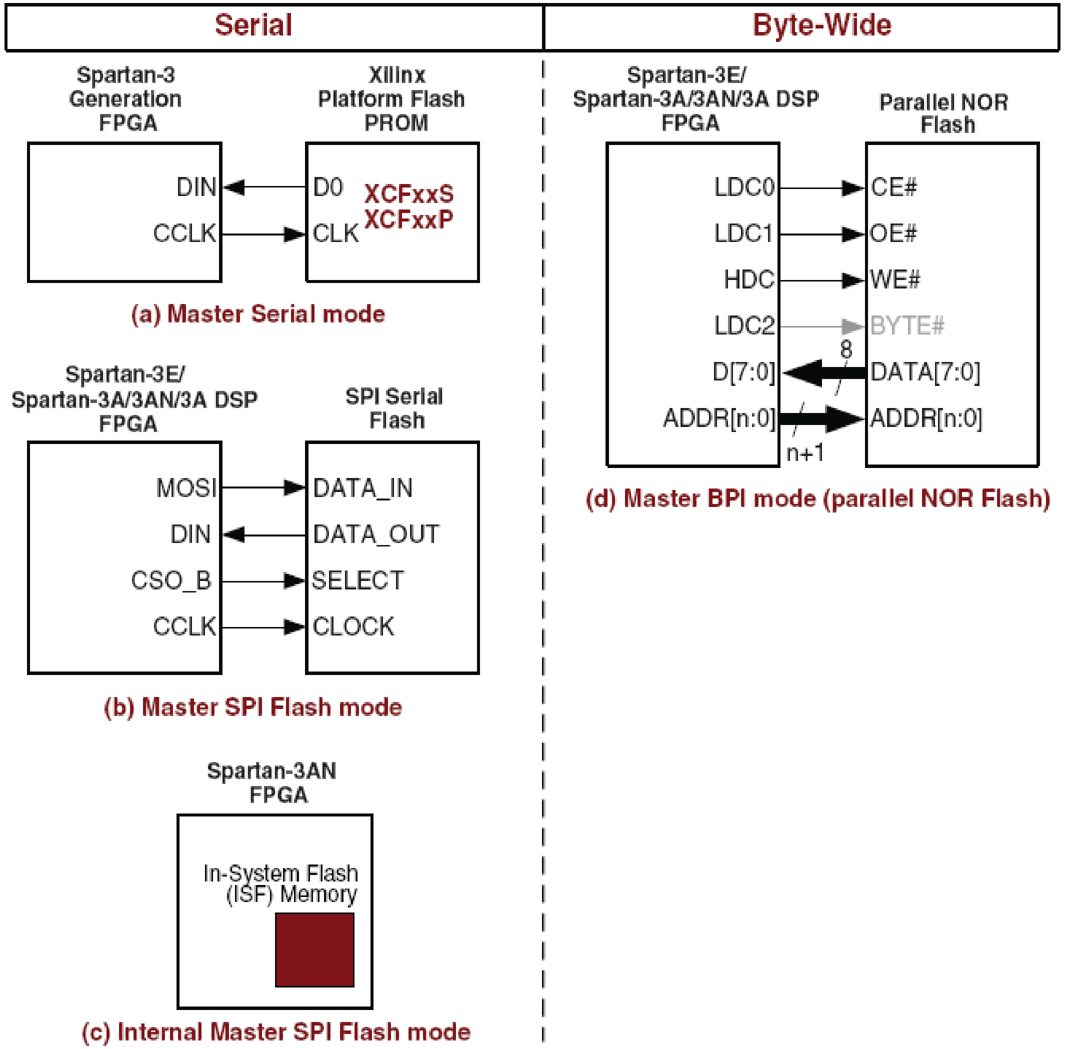
The Xilinx 7 Series FPGAs

- Industry's Lowest Power and First Unified Architecture
  - Spanning Low-Cost to Ultra High-End applications
- Three new device families with breakthrough innovations in power efficiency, performance-capacity and price-performance

	ARTIX 7	KINTEX 7	VIRTEX 7
	Lowest Power & Cost	Industry's Best Price/Performance	Industry's Highest System Performance
Logic Cells	20K – 355K	30K – 410K	285K – 2,000K
DSP Slices	40 – 700	120 – 1540	700 – 3,960
Max. Transceivers	4	16	80
Transceiver Performance	3.75Gbps	6.6Gbps 10.3Gbps	10.3Gbps 13.1Gbps 28Gbps
Memory Performance	800Mbps	2133Mbps	2133Mbps
Max. SelectIO™	450	500	1200
SelectIO™ Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below

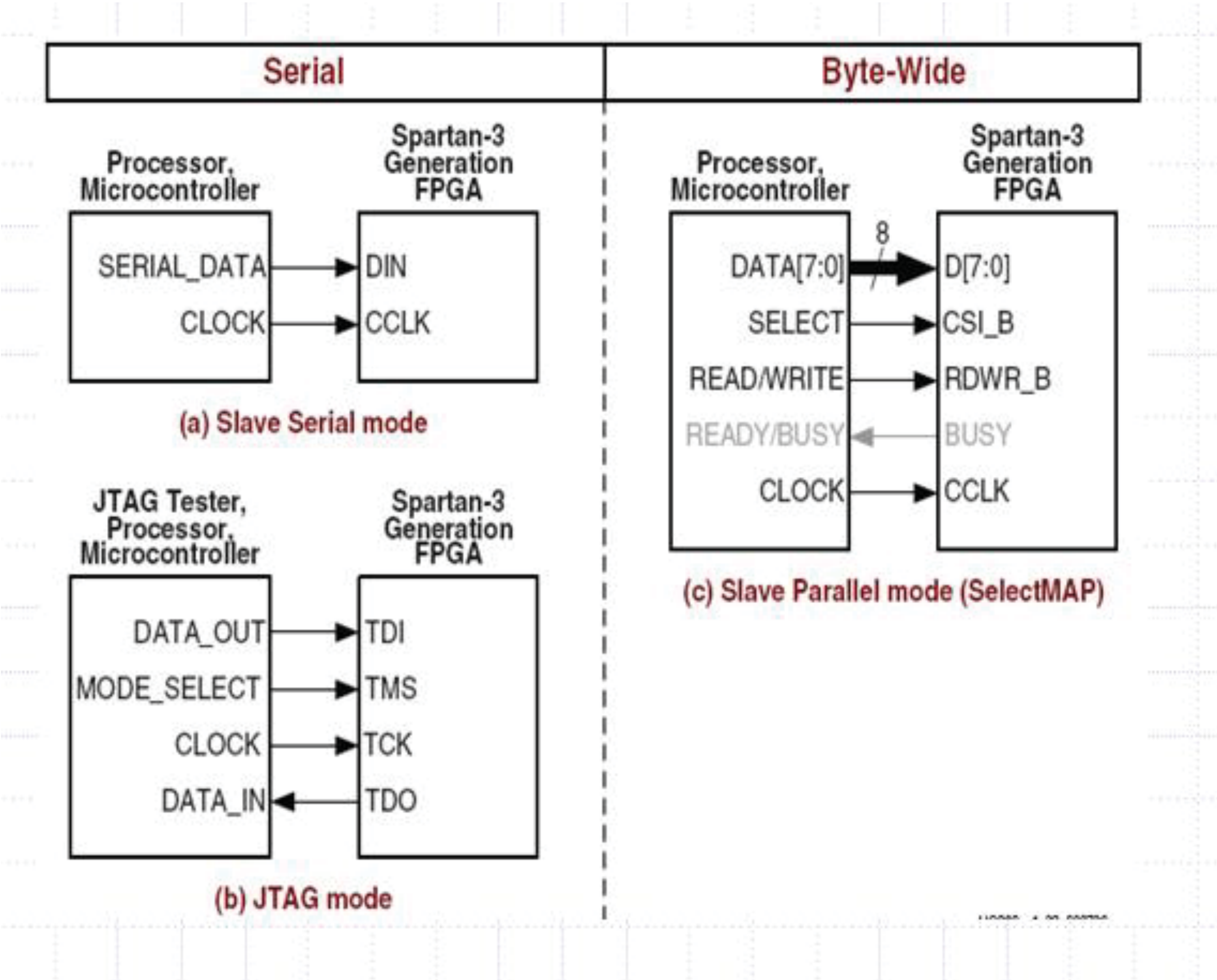
FPGA Configuration

FPGA Master



Serial
Byte-Wide
Spartan-3 Generation FPGA
Xilinx Platform Flash PROM
DIN
CCLK
D0
CLK
XCFxxS
XCFxxP
(a) Master Serial mode
Spartan-3E/ Spartan-3A/3AN/3A DSP FPGA
SPI Serial Flash
MOSI
DIN
CSO_B
CCLK
DATA_IN
DATA_OUT
SELECT
CLOCK
(b) Master SPI Flash mode
Spartan-3AN FPGA
In-System Flash (ISF) Memory
(c) Internal Master SPI Flash mode
Spartan-3E/ Spartan-3A/3AN/3A DSP FPGA
Parallel NOR Flash
LDC0
LDC1
HDC
LDC2
D[7:0]
ADDR[n:0]
CE#
OE#
WE#
BYTE#
DATA[7:0]
ADDR[n:0]
8
n+1
(d) Master BPI mode (parallel NOR Flash)

FPGA Slave


Serial
Byte-Wide
Processor, Microcontroller
Spartan-3 Generation FPGA
SERIAL_DATA
DIN
CLOCK
CCLK
(a) Slave Serial mode
JTAG Tester, Processor, Microcontroller
Spartan-3 Generation FPGA
DATA_OUT
TDI
MODE_SELECT
TMS
CLOCK
TCK
DATA_IN
TDO
(b) JTAG mode
Processor, Microcontroller
Spartan-3 Generation FPGA
8
DATA[7:0]
D[7:0]
SELECT
CSI_B
READ/WRITE
RDWR_B
READY/BUSY
BUSY
CLOCK
CCLK
(c) Slave Parallel mode (SelectMAP)