The Abdus Salam International Centre for Theoretical Physics

smr2499

International Training Workshop on FPGA Design for Scientific Instrumentation and Computing

11 November – 22 November 2013

Trieste – Italy

LABORATORY EXERCISES II

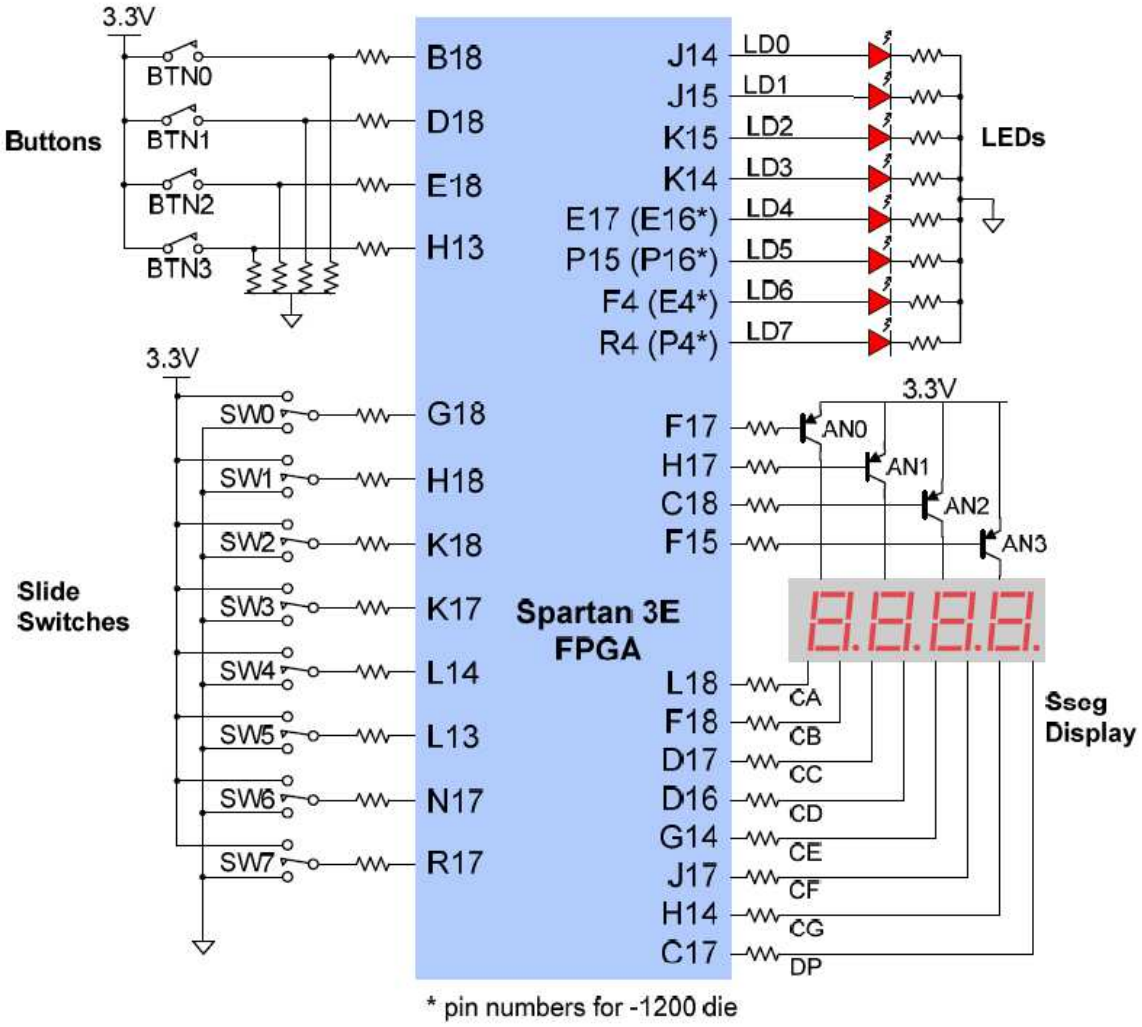
COMBINATIONAL AND SEQUENTIAL LOGIC DESCRIBED in VHDL

Logic Synthesis and FPGA Implementation

ICTP Multidisciplinary Laboratory
MLAB

Objective

- Implementation of your designs in the *FPGA Spartan 3E of the Nexys 2 board* (see I/O in figure below and user guide for more details).
- Writing and Utilization of *User Constraints Files* (.ucf)



Exercise 8

a) Design and Synthesize a Clock Divider that allows generating 1 Hz, 2 Hz, 5 Hz and 10 Hz clocks from the on-board 50 MHz clock. Use the on-board LEDs to show each one of the generated clocks.

b) Write the corresponding user constraints file, configure the FPGA, and test your design.

Exercise 9

a) Implement on the FPGA the *hexadecimal to 7-segment decoder* designed in exercise 3. Use the on-board SW0-SW3 switches and the display controlled by pin F15.
b) Write the corresponding user constraints file, configure the FPGA, and test your design.

Exercise 10

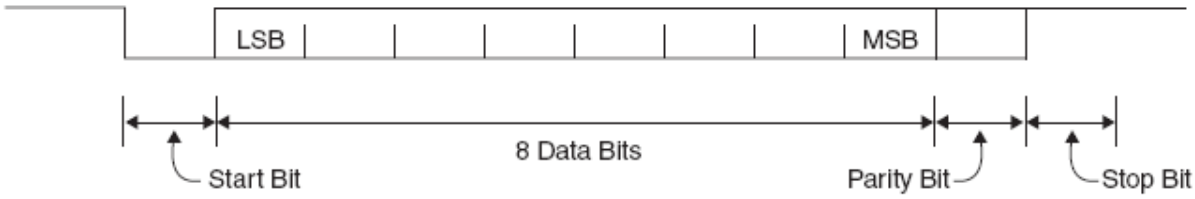
a) Implement on the FPGA the system designed in exercise 6. Use a common reset to initialize the counters, and the *switches* available in the board for the up/down input to define the counting mode of each counter. Use the available *buttons* for the *select* signal, and one of the *7-segment display* for visualization.
b) Write the corresponding user constraints file, configure the FPGA, and test your design.

Exercise 11

a) Implement on the FPGA the system designed in exercise 7 (part a).
b) Write the corresponding user constraints file, configure the FPGA, and test your design.

Exercise 12

1) Design a system for serial data transmission according to the RS-232 protocol. The format of the data to be transmitted is described in the figure below:



RS-232 formato de transmisión

a) Set the reception/transmission frequency at 9600 baud.
b) Transmit your first name that will be defined as a constant.

2) Write the corresponding user constraints file, configure the FPGA, and test your design (use the figure below as reference).