Advanced Training Course on FPGA Design and VHDL for Hardware Simulation and Synthesis

26 October - 20 November, 2009

VHDL & FPGA Architectures
Programmable Logic and VHDL Architectures

Nizar Abdallah
ACTEL Corp. 2061 Stierlin Court Mountain View
CA 94043-4653
U.S.A.
Lectures:
VHDL & FPGA Architectures
Outline

- Introduction to FPGA & FPGA design flow
- Synthesis I – Introduction
- Synthesis II - Introduction to VHDL
- Synthesis III - Advanced VHDL
- Design verification and timing concepts
- Programmable logic & FPGA architectures
- Actel ProASIC3 FPGA architecture
- System-on-Chip concepts
Programmable Logic and FPGA Architectures
It’s All About the Original Idea
PLD Market Growth

Billions of Dollars and Revenue Growth

<table>
<thead>
<tr>
<th>Year</th>
<th>Revenue</th>
<th>Growth</th>
</tr>
</thead>
<tbody>
<tr>
<td>2002</td>
<td>$156</td>
<td>1.4%</td>
</tr>
<tr>
<td>2003</td>
<td>$178</td>
<td>14.5%</td>
</tr>
<tr>
<td>2004</td>
<td>$222</td>
<td>24.6%</td>
</tr>
<tr>
<td>2005</td>
<td>$235</td>
<td>5.7%</td>
</tr>
<tr>
<td>2006</td>
<td>$260</td>
<td>10.7%</td>
</tr>
<tr>
<td>2007</td>
<td>$276</td>
<td>6.4%</td>
</tr>
<tr>
<td>2008</td>
<td>$299</td>
<td>8.2%</td>
</tr>
<tr>
<td>2009</td>
<td>$306</td>
<td>2.2%</td>
</tr>
<tr>
<td>2010</td>
<td>$326</td>
<td>6.7%</td>
</tr>
<tr>
<td>2011</td>
<td>$352</td>
<td>7.7%</td>
</tr>
</tbody>
</table>

Revenue CAGR 06/11 = 5.1%

Source: Gartner Dataquest Estimates (May 2007)
New adopters are in high volume segments
- Consumer grows from 8% to 15%
- Automotive grows from 1% to 6%

Traditional ASIC-crossover segments also growing well
- Industrial is up 9%
- Mil/Aero is up 2%

While high-end FPGA markets decline in share
- Comm down 15% in share
- Data proc down 8% in share
Cost: The exploding ASIC NRE

- Wafers today are worth from US $10 million to $100 million
- Amortize the $5 billion investment in a fab over a 5 year schedule costs > $3 million/day
- Equipment running all the time
- Must produce a semiconductor product in volumes of at least 5000 to 10 000 wafers per month
Cost: The exploding ASIC NRE

Source: Dataquest
Technology Advances vs. Crossover Volume

ASIC Costs
Start higher, but slope is flatter

For each technology advance, crossover volume moves higher

Total cost

Volume K units

FPGA .25μ
FPGA .15μ
ASIC .25μ
ASIC .15μ
New products are taking less time to go into volume. At the same time, new products also stay in volume for shorter
Missing a market window, because of a long development/debugging cycle can have a profoundly negative effect on the profitability of a product over its life.

Late market entry has a larger effect on profits than development cost overruns or a product price that is high.
Cost: System Re-configurability

- Lack of re-configurability in ASICs is a huge opportunity
- FPGAs offer flexible life cycle management

![Diagram showing market window comparison between reconfigurable and non-reconfigurable systems.](image-url)
Volume Requirement for ASICs

> 50% of the market available today for FPGAs

Source: IMS 2000
FPGA can address a very large part of the market today
FPGA can address a very large part of the market today
Performance Requirement for FPGAs

Maximum On-Chip Clock Frequencies (Megahertz) — FPGA Design Starts

Source: Gartner Dataquest (January 2003)

- FPGA can address a very large part of the market today

~75% ~25%
7 years ago, FPGAs were only gates & routing
\sim 25000 \text{ gates}

Today, there are several system-level features.
\sim 5,000,000 \text{ gates}

The trend to add more IP in FPGAs continues
A Brief History…

Once upon the time, there were… ROMs:

- **Expensive**
  - Need for creating an application specific mask set by the vendor

- **Long development cycle**
  - Changes = New mask set by the vendor
PROMs: Programmable Read Only Memories

✔ First field programmable devices

✖ Slow access time
  ➤ Not useful for applications where speed is an issue

✖ Limited number of inputs

✖ Require different technology
  ➤ Extra masks
  ➤ Extra processing steps
  ➤ Extra development time
  ➤ Extra cost
PLAs: Programmable Logic Arrays

- Classified as a simple programmable logic device (SPLD)
- The first programmable logic device introduced in the early 1970s by Philips.
- Based on the idea that logic functions can be realized in sum-of-products form.
- A programmable AND array followed by a programmable OR array.

- HDLs to convert Boolean equations into connections
  - ABEL
  - PALASM
PLAs: Programmable Logic Arrays

A Brief History...

PLAs (Programmable Logic Arrays):
- **Inputs**
  - A
  - B
  - C
- **AND Plane**
  - Fuse intact
  - Fuse blown
- **OR Plane**
- **Outputs**
- **PLA Architecture**
PALs: Programmable Array Logic

- A device similar to PLA.
- Introduced to overcome the weaknesses of PLAs at that time (programmable switches were hard to fabricate correctly and introduced significant propagation delays).
- A programmable AND array followed by a fixed OR array. Inverters at the inputs and outputs.
- HDLs to convert Boolean equations into connections
  - ABEL
  - PALASM
PALs: Programmable Array Logic
First idea of an FPGA/CPLD different from a PLD:

- 1984: Ross Freeman / Zilog, Inc.
  - Xilinx, Inc. with $4.25M in venture capital

- 1983: Altera Corp.

- 1985: Actel Corp. with FPGAs based on antifuse switching elements
Large number of PALs in a single chip

CPLD Architecture (Altera)
Complex Programmable Logic Devices (CPLDs)

Function Block

- Typically similar to a PAL architecture
- Same technology and programming tools than a PAL
- Additional specialized logic in each FB: XOR (difficult in a PAL), Muxes, FFs…
- Additional embedded devices in the CPLD:
  - SRAM and Flash memories
  - Microcontrollers and microprocessors
  - Digital Signal Processors (DSPs)
  - Phased Locked Loops (PLLs)
  - Network processors
Selection criteria

- The programming technology
  - Equipment for device programming

- The FB capability
  - #FFs, #inputs, built-in XORs …

- The number of FB in the device

- The kind of FF control available

- Embedded devices

- The number and type of IO pins

- The number of clock input pins
What is an FPGA?

- Field Programmable Gate Array

A large number of logic gates in an IC array that can be connected (configured) electrically

The Four Components of FPGAs
- The Configuration Element
- The Logic Module
- The Memory
- Control Circuits/Special Features
The Key Element of an FPGA

The Interconnect Switch

XXX
FPGA Technologies Compared

<table>
<thead>
<tr>
<th>Technology</th>
<th>Reprogrammable</th>
<th>Best of Both Worlds Reprogrammable &amp; Nonvolatile</th>
<th>Nonvolatile</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>Large Switch</td>
<td>Small Switch</td>
<td>Smallest Switch</td>
</tr>
<tr>
<td></td>
<td>expensive wires</td>
<td>cheap wires</td>
<td>cheapest wires</td>
</tr>
<tr>
<td></td>
<td>Low Logic Utilization</td>
<td>High Logic Utilization</td>
<td>Highest Logic Utilization</td>
</tr>
<tr>
<td></td>
<td>typ 60%</td>
<td>typ &gt;85%</td>
<td>typ &gt;90%</td>
</tr>
</tbody>
</table>

© 2005 Nizar Abdallah
Flash Switch

ProASIC, ProASIC<sup>Plus</sup>, ProASIC III Routing Switch
Types of FPGAs (*Switch*)

**Volatile** (loses its configuration when power is turned off)
- Reprogrammable: **SRAM** process and device technology
  - Xilinx, Altera, Lattice

**Non-Volatile** (keeps its configuration)
- **One Time Programmable (OTP):** **Anti-fuse**
  - Actel, Quicklogic
- **Reprogrammable:** **Flash**
  - Actel
Regular array of logic

Control Store

110101011101010010001
Configurable logic blocks
Selection criteria

- Programming technology
- Configurable logic block
  #FFs, #inputs, …
- The number of logic blocks in the device
- Embedded devices
- The number and type of IO pins
- The number of clock input pins
## CPLD or FPGA?

<table>
<thead>
<tr>
<th></th>
<th>CPLD</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Architecture</strong></td>
<td>PAL-like</td>
<td>Gate array like</td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>Fast, predictable</td>
<td>Application dependent</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>Low to medium</td>
<td>Medium to high</td>
</tr>
<tr>
<td><strong>Interconnect</strong></td>
<td>Crossbar</td>
<td>Routing</td>
</tr>
<tr>
<td><strong>Power consumption</strong></td>
<td>High per gate</td>
<td>Low per gate</td>
</tr>
</tbody>
</table>
Specifications

- External block diagram (chip in the system)
- Internal block diagram
- Description of the IO pins
- Timing & power constraints
  - Clock frequency, external setup, external hold, ...
- Gate count estimate
- Package type
- Price target
- Test procedure
Choosing Device and Tools

- Synthesis
  - Coding style for the HDL
- ...
Design

- Partitioning ⇒ Implementation ⇒ Assemblage
- Top-down flow
- Work with the device architecture
- Do synchronous design
- Protect against metastability
- Avoid floating nodes
- VERIFY AT EACH STEP
CPLD/FPGA Design Methodology

Verification

- Simulation
- Design review
- Timing analysis
- Power analysis
- Formal verification